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MediaLB Interface Test Bench V2.2.X User Manual

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MediaLB Interface Test Bench

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Document History

Version	Date	Section	Comment on Changes
V2.2.X-1	2011-12-09	2.3	Functional Restrictions: Max. Synchronous Bandwidth is 15 quadlets.
		6.2	Split Test Status Fields for all data types. Updated screen shots. Added value range for parameters.
		7.2.1	Update MDP Packet Format description and drawing.
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		5	Added: Flashing of MITB Platform
		6.2	Additional GUI parameters defined
		7.4	Index for data bytes modified in Figure 7-6: Isochronous Packet Format
		8	Additional test cases defined
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		Appendix C	Spare Part List modified
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1 Preface

1.1 Intended Use

This SMSC product is intended to be used for developing, testing or analyzing MOST® and MediaLB® based multimedia products and systems by persons with experience in developing multimedia devices.

Notice Use this SMSC product only with original SMSC devices, e.g., provided power supply. Do not interfere in the product's original state. Otherwise user safety, faultless operation and electromagnetic compatibility are not guaranteed.
To avoid electric shocks and short circuits use this device only in an appropriate environment.
This open device may exceed the limits of electromagnetic interference. Electromagnetic compatibility can be only achieved if the equipment is built into an appropriate housing.

1.2 Scope of Delivery

The delivery of the MediaLB Interface Test Bench (MITB) consists of:

- 1 x MITB Platform
- 2 x Physical+ Interface Board OS81110 (Variant 1)
- 1 x Physical+ Interface Board OS81110 (Variant 3)
- 1 x RS232 cable
- 1 x USB-RS232 Adapter
- 1 x Ethernet crossover cable
- 1 x Optical cable set
- 1 x Power supply
- 1 x Installation CD including:
  - MITB Graphical User Interface (GUI)
  - PCFlasher application
  - MITB FPGA image
  - PowerPC Pattern Generator & Analyzer firmware
  - MITB OS81110 test firmware
  - MITB user manual
  - Physical+ Interface Board OS81110 data sheet
  - MediaLB Analyzer product flyer and user manual
  - INIC Explorer product flyer and user manual

Check your shipment for completeness.
If you have any complaints direct them to sales-ais-europe@smsc.com (Europe and Asia) or to sales-ais-usa@smsc.com (America). Providing the delivery note number eases the handling.

Hint Optional tools such as INIC Explorer and MediaLB Analyzer are not part of the MITB deliverables and must be purchased separately.

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2 Introduction

The MediaLB Interface Test Bench (MITB) represents a hardware platform used to verify the link-layer implementation of a MediaLB device. Verification is based on the loop-back functionality of the MediaLB Device Under Test (MDUT) and test patterns, required to check for a proper implementation. Test patterns are generated by the Pattern Generator & Analyzer (PGA) software, which is an integral part of the MITB.

For a test, the MDUT might be connected to the test bench. The PGA generates the test patterns and transmits them over the MediaLB Port to be received by the MDUT. The loop-back functionality provided on the MDUT needs to facilitate reception and re-transmission of the test patterns. The re-transmitted test patterns are received by the MITB and verified against the transmitted patterns.

To verify proper operation of a MediaLB device, the MITB supports various test modes and parameters including MediaLB port configurations and data types. Typical parameters for the port configuration are: MediaLB interface mode (3-Pin or 6-Pin), MediaLB clock speed (256xFs, 512xFs, 1024xFs…) and transferred data types (control message data, asynchronous packet data, synchronous and isochronous data).

The MITB provides an RS232 interface to a host PC. A Graphical User Interface (GUI) runs on the PC and is able to configure the generated test patterns and to display the test results of the pattern verification.

2.1 Overview

A complete hardware setup, used to verify if a MediaLB device has been implemented properly typically includes user hardware and a MITB, both parts connected. The MediaLB device to be tested is part of the user hardware (see for example Figure 2-1 and Figure 2-2). To simplify the verification of proper MDUT functionality, the MITB features a PGA. The patterns, generated by the PGA are transmitted by the MITB. The MDUT receives these patterns on its MediaLB Port and re-transmits the same patterns which in turn are received by the MITB and verified by the PGA. If the data patterns transmitted and received by the MITB are identical, it can be ensured that the MDUT is able to properly receive and transmit data on the MediaLB interface.

Since the test pattern generation and analysis is done by the MITB, the implementer of the MDUT can focus on programming the MDUT rather than spend time and resources to configure the MediaLB Controller. In addition, the user is exempt from coding a pattern generator and analyzer.

To be able to implement a sophisticated PGA the MITB Platform features an FPGA incorporating a PowerPC and a MediaLB device interface. The PowerPC generates and analyzes the test patterns for all MediaLB data types including control, asynchronous, synchronous and isochronous data. The MediaLB device interface realizes the hardware port required to transmit and receive the data patterns on MediaLB.

The PowerPC is linked to a host PC via an RS232 interface. A GUI, running on the host PC, allows the configuration of the generated test patterns, as well as the configuration of the MediaLB controller (INIC) connected to the MDUT and enables the visualization of pattern verification results and error reporting.

In addition to the GUI, the MITB Platform features a LCD display and LEDs to provide status information like MOST and MediaLB Lock conditions.

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An optical MOST150 network is used as connection between the user hardware and the MITB Platform. On the MITB Platform, the MOST150 interface is realized by a special add-on-card also referred to as Physical+ Interface Board OS81110[1] which features an OS81110 MOST150 transceiver as well as a MOST150 2+0 Fiber Optic Transceiver (FOT) unit. The FPGA on the MITB Platform and the OS81110 on the Phy+ Board are connected via a MediaLB 6-Pin interface.

The user hardware also needs to have a MOST150 interface. Dependent on the available user hardware this can be done by the Phy+ Board or by integrating an OS81110 MOST150 transceiver and the FOT unit on the user hardware.

Based on different types of user hardware, the MITB can be arranged as:

- MediaLB Device Setup (see section 2.1.1) or
- MOST150 Device Setup (see section 2.1.2)

The MediaLB Device Setup is applicable when the user provides a MediaLB device without a MOST interface. If the user owns a MOST150 device with an integrated MDUT as well as an MOST150 transceiver and an optical MOST150 interface, it is recommended to use the MOST150 Device Setup. Both setups are described in detail in the following sections.

Regardless which setup is used, in both cases the OS81110 transceiver connected to the MDUT is configured remotely by the GUI running on the host PC via the MOST network. This is required to configure the complete setup for a dedicated test case and to relief the user from configuring the OS81110.

The OS81110 connected to the MDUT needs to be flashed with a dedicated MITB OS81110 test firmware, which allows remote configuration and the generation of specific test scenarios. By default, the Phy+ Boards delivered with the MITB are flashed with this firmware. An INIC Explorer [1] is required in case these Phy+ Boards need to be flashed with a firmware different than the MITB OS81110 test firmware. This may be required when the Phy+ Boards are re-used for other applications than the MITB or the MOST150 Device Setup is used and the OS81110 on the user hardware needs to be flashed with the MITB OS81110 test firmware.

To complete the entire setup, a MediaLB Analyzer [2] can be connected to the MediaLB interface of the MDUT. This is highly recommended and required for observing the data transfer on the MediaLB interface between the MDUT and the connected INIC and to debug error cases.

To be able to connect the MediaLB Analyzer, a MediaLB 3/6-Pin high-speed debug header is required. Using the MOST150 Device Setup, this connector needs to be implemented on the user hardware. If a Phy+ Board is used, as required for the MediaLB Device Setup, the MediaLB debug connector is available on the Phy+ Board.

Hint INIC Explorer [1] as well as MediaLB Analyzer [2] are not part of the MITB delivery and need to be purchased separately.

[1] Hereafter abbr. as Phy+ Board

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2.1.1 MediaLB Device Setup

The following figure outlines the block diagram of the MediaLB Device Setup.

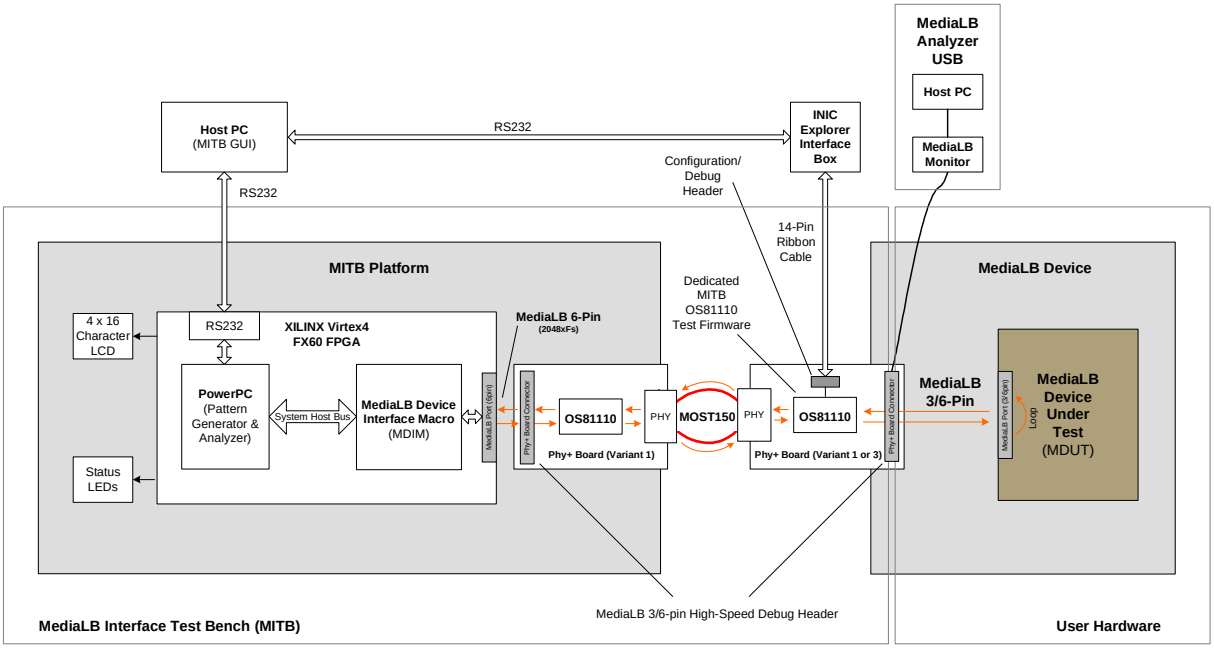

Figure 2-1: MediaLB Device Setup

At this setup the user hardware is realized by a MediaLB device, which needs to integrate the MDUT as well as a MediaLB 3/6-Pin high-speed debug header, used to connect a Phy+ Board. The Phy+ Board connected to the user hardware is required to realize the above outlined setup.

Given that the Phy+ Board connected to the user's MediaLB device is part of the MITB, two interfaces are provided by the MITB configured as MediaLB Device Setup:

- RS232 interface
  - Main interface to the GUI running on the host PC
  - Enables configuration of PGA software and definition of generated test patterns
  - Used to pass test results to the host PC

- MediaLB 3/6-Pin interface on high-speed debug header of Phy+ Board connected to the user's MediaLB device
  - Supports single-ended MediaLB 3-Pin interface
  - Supports differential MediaLB 6-Pin interface
  - Used to connect MDUT
  - Optionally used to connect MediaLB Monitor for MediaLB interface analysis

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Additionally, the MITB provides the following main components:

- XILINX Virtex4 FX60 FPGA including:
  - PowerPC used to run the PGA
  - MediaLB Device Interface Macro featuring a differential MediaLB 6-Pin port
  - RS232 interface for connection to host PC
- 1st Phy+ Board (Variant 1)
  - Connected to MITB Platform
  - Incorporates an OS81110 MOST150 transceiver
  - Connected via MediaLB 6-Pin interface (operated at 2048xFs) to FPGA
  - Serves as gateway between the MediaLB 6-Pin port of the FPGA on the MITB Platform and the MOST150 network
- 2nd Phy+ Board (Variant 3)
  - Connected to user hardware
  - Optimized for a single-ended MediaLB 3-Pin interface
  - Used for testing of MediaLB 3-Pin port of MDUT
  - Connected via MediaLB 3/6-Pin high-speed debug header to MDUT
  - Serves as gateway between the MOST150 network and the MDUT
  - Optically connected to 1st Phy+ Board
- 3rd Phy+ Board (Variant 1)
  - Connected to user hardware
  - Optimized for a differential MediaLB 6-Pin interface
  - Used for testing of MediaLB 6-Pin port of MDUT
  - Connected via MediaLB 3/6-Pin high-speed debug header to MDUT
  - Serves as gateway between the MOST150 network and the MDUT
  - Optically connected to 1st Phy+ Board
- LCD Display
  - Provides information on the PGA version running on the MITB Platform
- Status LEDs for:
  - MOST Lock detection
  - MediaLB Lock detection
  - Power indication

Note For testing the MediaLB 3-Pin or 6-Pin port of a MDUT different Phy+ Boards are required:
- MediaLB 3-Pin port testing requires Phy+ Board Variant 3 (2nd Phy+ Board).
- MediaLB 6-Pin port testing requires Phy+ Board Variant 1 (3rd Phy+ Board).

The requirements for the user hardware realizing a MediaLB device are described in section 2.5.1.

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2.1.2 MOST150 Device Setup

The following figure outlines the block diagram of the MOST150 Device Setup

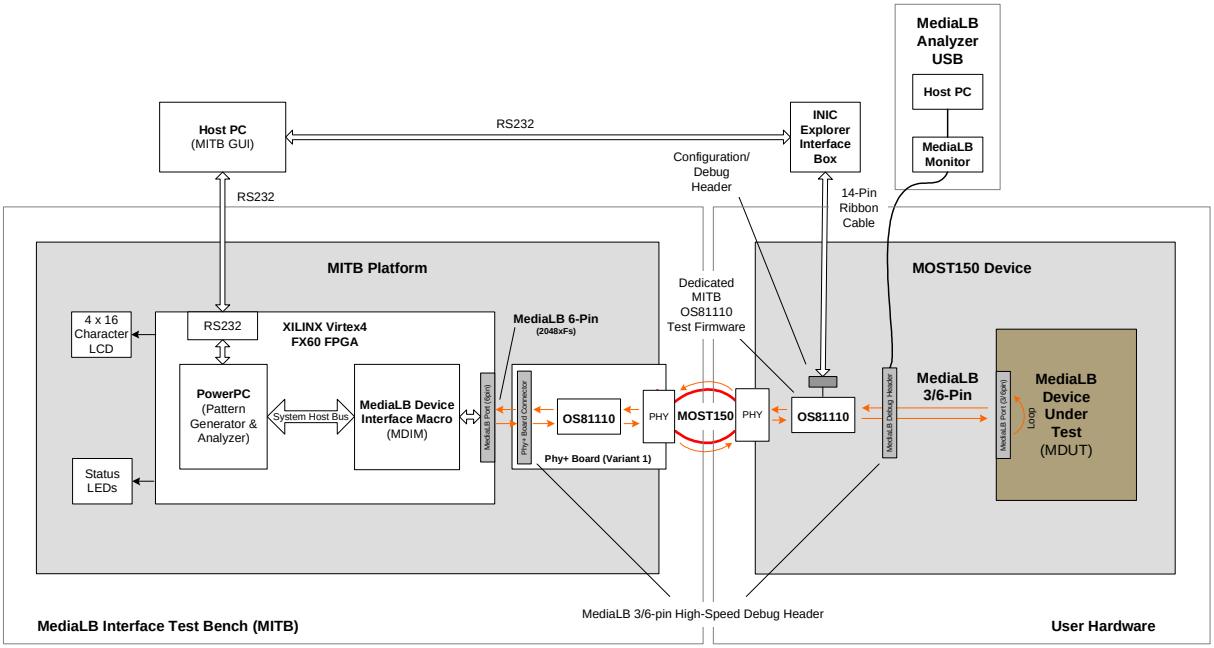

Figure 2-2: MOST150 Device Setup

The MOST150 Device Setup is applicable in case the user hardware is realizing a MOST150 device. This requires that on the user hardware the MDUT is integrated as well as an OS81110 MOST150 transceiver chip and an optical MOST150 network interface. The MITB and the user hardware are connected via an optical MOST150 network. A MediaLB 3-Pin and/or a 6-Pin interface is used to connect the MDUT and the OS81110 INIC/MediaLB controller on the user hardware.

Configured as a MOST150 Device Setup, the MITB provides two main interfaces:

- RS232 interface
  - Main interface to the GUI running on the host PC
  - Enables configuration of PGA software and definition of generated test patterns
  - Used to pass test results to host PC
- Optical MOST150 interface
  - Realized by a Phy+ Board
  - Used to connect customer MOST150 device which incorporates MDUT

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Additionally, the MITB provides the following main components:

- XILINX Virtex4 FX60 FPGA including:
  - PowerPC used to run the PGA
  - MediaLB Device Interface Macro featuring a differential MediaLB 6-Pin port
  - RS232 interface for connection to host PC
- Phy+ Board (Variant 1)
  - Connected to MITB Platform
  - Incorporates an OS81110 MOST150 transceiver
  - Connected via MediaLB 6-Pin interface (operated at 2048xFs) to FPGA
  - Serves as gateway between the MediaLB 6-Pin port of the FPGA and the MOST150 network
- LCD Display
  - Provides information on the PGA version running on the MITB Platform
- Status LEDs for:
  - MOST Lock detection
  - MediaLB Lock detection
  - Power indication

The requirements for the user hardware realizing a MOST150 device are described in section 2.5.2.

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2.2 Features

2.2.1 General Features

- Hardware setup to verify link-layer implementation of a MediaLB device
- Test pattern generation and verification of the following data types:
  - Control messages
  - Asynchronous packets
  - Synchronous streaming data
  - Isochronous packets
  - Combination of the above listed data types
- Generation of the following MediaLB commands:
  - *NoData*
  - *SyncData*
  - *AsyncStart, AsyncContinue, AsyncEnd, AsyncBreak*
  - *ControlStart, ControlContinue, ControlEnd, ControlBreak*
  - *IsoNoData, Iso4Bytes, IsoSync4Bytes*
  - *MOSTLock, MOSTUnlock, MLBReset*
- Generation of the following MediaLB RxStatus responses:
  - *ReceiverReady*
  - *ReceiverBusy*
  - *ReceiverBreak*
  - *ReceiverProtocolError*
- Supported Setups:
  - MediaLB Device Setup
  - MOST150 Device Setup
- Optical physical layer for MOST150 supported
- MITB operates as MediaLB controller and MOST150 network master
- GUI for test pattern configuration
- GUI for remote configuration of MediaLB controller (INIC) connected to MDUT
- GUI for test status visualization

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2.2.2 Hardware Features

- Supported physical MediaLB interfaces:
  - Single-ended MediaLB 3-Pin interface
  - Differential MediaLB 6-Pin interface
- Supported MediaLB debug headers:
  - MediaLB 3/6-Pin high-speed debug header (SAMTEC 0.5 mm, 20 pair, high-speed, differential pair socket QSH-020-01-L-D-DP-A)
- Supported MOST Phy+ Boards:
  - Phy+ Board – Variant 3 (optimized for single-ended MediaLB 3-Pin interface)
  - Phy+ Board – Variant 1 (optimized for differential MediaLB 6-Pin interface)
- Supported MediaLB clock rates on 3-Pin interface:
  - 256xFs (e.g., 256 x 48 kHz = 12.288 MHz)
  - 512xFs (e.g., 512 x 48 kHz = 24.576 MHz)
  - 1024xFs (e.g., 1024 x 48 kHz = 49.152 MHz)
- Supported MediaLB clock rates on 6-Pin interface:
  - 2048xFs (e.g., 2048 x 48 kHz = 98.304 MHz)
  - 3072xFs (e.g., 3072 x 48 kHz = 147.446 MHz)
  - 4096xFs (e.g., 4096 x 48 kHz = 196.608 MHz)
- Status LEDs for:
  - MediaLB Lock detection
  - MOST Lock detection
  - Power indication
- RS232 interface to host PC
- 10/100 Ethernet interface to host PC for flashing the MITB platform
- Trigger connector for generation of error events

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2.2.3 Software (GUI & PGA) Features

- GUI is split in specific functional sections including:
  - Configuration tab (6.2.1)
  - Control tab (6.2.2)
  - Asynchronous tab (6.2.3)
  - Synchronous tab (6.2.4)
  - Isochronous tab (6.2.5)
  - System Commands tab (6.2.6)

- Configuration:
  - Manual as well as script-based configuration of test cases
  - Optional configuration and debug message log windows
  - Optional generation of error trigger events
  - DUT MOST Target Address
  - RS232 port

- Supported test pattern parameters:
  - Control data test:
    - Tx/Rx ChannelAddress
    - Message length
    - Test duration
    - Pattern type
    - Throughput
  - Asynchronous data test:
    - Tx/Rx ChannelAddress
    - Blockwidth in quadlets per frame
    - Packet length
    - Test duration
    - Pattern type
    - Packet delay
    - Asynchronous packet type (MDP/MEP)
    - MEP destination and source address
  - Synchronous data test:
    - Tx/Rx ChannelAddress
    - Blockwidth in quadlets per frame
    - Pattern type
  - Isochronous data test:
    - Tx/Rx ChannelAddress
    - Blockwidth in quadlets per frame
    - Packet length
    - Test duration
    - Pattern type
    - Throughput
  - System command test:
    - Generation of MOSTLock, MOSTUnlock and MLBReset commands

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- Test result reporting
  - Number of transmitted messages/packets
  - Number of received messages/packets
  - Number of errors
  - Number of locks
  - Throughput
  - Result reporting done by visualization in GUI as well as test protocol file

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2.3 Functional Restrictions

The following limitations apply to the MITB:

- The PGA supports generation and analysis of control messages, asynchronous packets and isochronous packets with the following lengths (total packet length including 2 bytes of PML).
  - Control messages
    - MCM: Min. message length of 19 bytes; max. message length of 58 bytes
  - Asynchronous packets
    - MDP: Min. packet length of 16 bytes; max. packet length of 1534 bytes
    - MEP: Min. packet length of 26 bytes; max. packet length of 1526 bytes
  - Isochronous packets
    - Packet length of 188 bytes and 196 bytes
- The PGA is able to generate and verify test patterns up to the following data quadlets per MOST/MediaLB frame (one direction).
  - Control messages
    - Max. 1 quadlet/frame
  - Asynchronous packets
    - Max. 27 quadlet/frame
  - Synchronous streaming data
    - Max. 15 quadlet/frame
  - Isochronous packets
    - Max. 27 quadlet/frame
- The MITB does not support the data transfer of multiple logical MediaLB channels with the same data type and direction (e.g., the transfer of two or more logical synchronous channels with the same direction is not supported).
- The MOST150 Device Setup: of the MITB described in section 2.1.2 is only possible if the MDUT is part of a MOST150 device incorporating an OS81110 MOST150 transceiver and an optical MOST150 interface.

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2.4 System and Tool Requirements

To setup a complete MITB several components are required. Some of them are compulsory others are optional.

2.4.1 Compulsory Components

For utilizing the MITB a host PC or laptop is needed. The following PC environment is recommended:

- Pentium Class PC
- 2 GB RAM
- 1 GB free disk space
- Three Free USB 2.0 ports
- Two free RS232 ports
- Windows XP or 2000

Additionally, the following SMSC components are required to setup a complete MITB:

- INIC Explorer Interface Box [1]
- OSS Flasher (free of charge) [2]

The INIC Explorer Interface Box and the OSS Flasher are required to flash the MITB OS81110 test firmware to the OS81110 connected to the MDUT. By default the Phy+ Boards, part of the MITB delivery, are flashed with the MITB OS81110 test firmware. If a firmware update is necessary or the Phy+ Boards are used on different applications than the MITB, it may be required to flash the OS81110 chips assembled on the Phy+ Boards. Flashing of the OS81110 connected to the MDUT is also necessary when using the MOST150 Device Setup with the OS81110 assembled on the user hardware.

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2.4.2 Optional Components

For debugging the MediaLB interface between the MITB and the MDUT, the following tools are recommended:

- MediaLB Analyzer [2]
- Oscilloscope

As outlined in Figure 2-1: MediaLB Device Setup and Figure 2-2: MOST150 Device Setup, the MediaLB Analyzer may be connected to the MediaLB 3/6-Pin high-speed debug header to visualize data transfer on the MediaLB interface between the MDUT and the connected OS81110 MediaLB controller. Additionally, the MediaLB Analyzer can also be connected to the MediaLB 3/6-Pin high-speed debug header on the MITB Platform to observe MediaLB data transfer between the FPGA and the connected OS81110.

The MediaLB Analyzer allows for seamless observation of transferred MediaLB data in raw data format on MediaLB protocol level and additionally, it enables visualization of combined and disassembled control messages as well as asynchronous packet data. It is highly recommended to use a MediaLB Analyzer to observe and debug data transfer occurring on the MediaLB interface of the MDUT.

To verify the signal integrity on the physical-layer of the MediaLB interface, an oscilloscope may be useful.

2.5 User Hardware Requirements

Dependent on the type of MITB setup (MediaLB Device Setup or MOST150 Device Setup) used, different requirements apply for the user hardware.

2.5.1 MediaLB Device Setup

To build-up the MITB as MediaLB Device Setup (see Figure 2-1: MediaLB Device Setup), the user needs to provide the following components and functionality on the user hardware:

- MediaLB 3/6-Pin Device Under Test (MDUT)
  - Connected to Phy+ Board connector via 3-Pin single-ended and/or 6-Pin differential MediaLB interface
  - Must provide loop-back functionality required to provide reception and re-transmission of test patterns
- Phy+ Board connector
  - Used to connect Phy+ Board (Variant 1 and 3)
  - Supports single-ended MediaLB 3-Pin interface (Phy+ Board Variant 3)
  - Supports differential MediaLB 6-Pin interface (Phy+ Board Variant 1)
  - Required to connect MediaLB Analyzer

For layout information on the Phy+ Board connector refer to section 3.6.

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2.5.2 MOST150 Device Setup

If the MOST150 Device Setup is used to verify the proper operation of the MDUT (see Figure 2-2: MOST150 Device Setup for details) the following components and functionality needs to be implemented on the user hardware:

- MediaLB 3/6-Pin Device Under Test (MDUT)
  - Connected to the OS81110 via 3-Pin single-ended and/or 6-Pin differential MediaLB interface
  - Must provide loop-back functionality to allow reception and re-transmission of test patterns
- OS81110 MOST150 INIC transceiver
  - Connected to MDUT via single-ended 3-Pin and/or differential 6-Pin MediaLB interface
  - Functions as MediaLB controller
  - Flashed with special MITB OS81110 test firmware
  - Functions as gateway between MOST network and MediaLB Port of MDUT
- Optical MOST150 interface
  - MOST150 2+0 Header
- MediaLB 3/6-Pin high-speed debug header
  - Required to connect MediaLB Analyzer for analysis of MediaLB data flow
- Configuration/debug header
  - Required to flash OS81110 MOST150 transceiver with dedicated MITB OS81110 test firmware or standard INIC firmware

For layout information on the MediaLB 3/6-Pin high-speed debug header and the configuration/debug header refer to section 3.6.

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2.6 Further Reading

This user manual describes the setup and usage of the MITB and its components.

For detailed information about the INIC Explorer Interface Box refer to the INIC Explorer User Manual [1].

For further information about the MediaLB Analyzer refer to the MediaLB Analyzer User Manual [2].

Information on the Physical+ Board OS81110 [3] is available in a data sheet and includes reference schematics required to realize an optical MOST150 interface as well as connector definitions.

Detailed information about the physical layer and link-layer of a MediaLB 3-Pin as well as 6-Pin interface can be found in the MediaLB Specification V4.1 [4].

Information on the MOST150 OS81110 transceiver is stated in the OS81110 data sheet [5] and the OS81110 INIC API User's Manual [6].

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3 Component Description

3.1 MediaLB Interface Test Bench Platform

The MITB platform represents the main hardware component of the MediaLB Interface Test Bench. The MITB platform comes with all components properly configured and is ready-to-use.

The following figure depicts the MITB platform and its main components, which are described below.

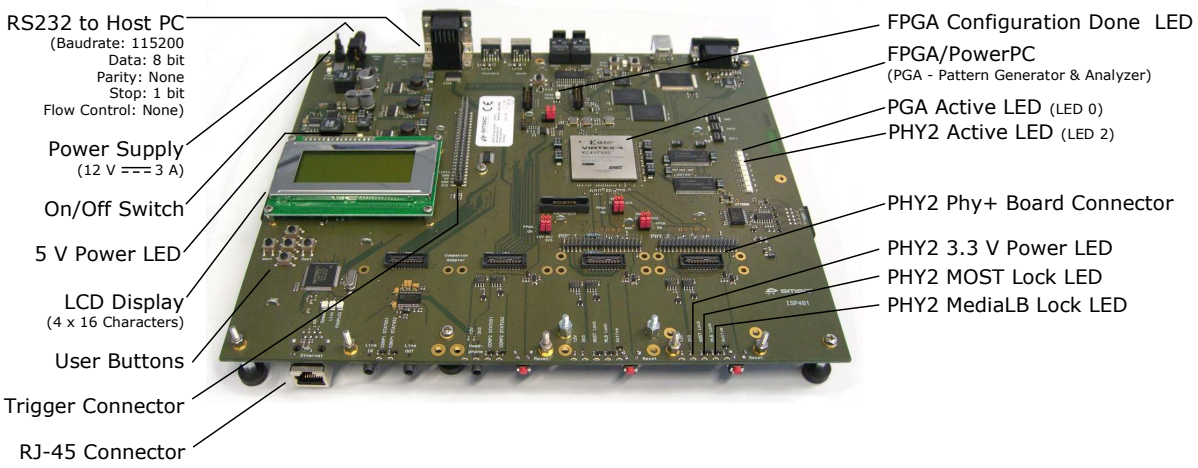

Figure 3-1: MediaLB Interface Test Bench Platform

RS232 to Host PC
The MITB platform features two 9-pin, female, D-SUB RS232 connectors. The lower one is used to establish an RS232 connection to a host PC. Via this connection the GUI running on the host PC communicates with the Pattern Generator & Analyzer on the MITB platform.

The RS232 interface is configured for the following parameters:

- Baudrate: 115200
- Data: 8 bit
- Parity: None
- Stop: 1 bit
- Flow Control: None

To enable communication with the MITB platform, the GUI running on the host PC automatically configures the RS232 port of the PC with the proper parameters.

Power Supply
The MITB platform is designed for a typical power supply of 12 V DC voltage and a power consumption of 3 A. A proper power supply is part of the MITB delivery.

On/Off Switch
The on/off switch is used to turn on and off the power supply of the MITB platform.

5 V Power LED
The 5 V Power LED indicates if the platform is properly powered.

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LCD Display
Status information such as version of the Pattern Generator & Analyzer firmware running on the platform is provided on the 4 x 16-character LCD display.

User Buttons
There are five active-high pushbutton switches available for general-purpose usage. The ***WEST*** button is used to initiate the flash process of the MITB platform. Refer to section 5 for details on how to flash the MITB platform.

Trigger Connector
For debugging purposes the MITB platform features an error trigger connector. See section 3.6.4 for details.

RJ-45 Connector
For flashing FPGA images and Pattern Generator & Analyzer software the MITB platform features an RJ-45 connector used to establish a 10/100 Ethernet connection to a host PC or laptop.

Refer to chapter 5 for details about flashing the MITB platform.

FPGA Configuration DONE LED
This LED illuminates when the FPGA on the MITB platform has been properly configured.

FPGA/PowerPC
The MITB Platform features a XILINX Virtex4 FPGA with integrated PowerPC. The PowerPC is used to run the Pattern Generator & Analyzer firmware. Additionally, the FPGA integrates a MediaLB 6-Pin interface.

PGA Active LED
This LED blinks periodically when the PGA is up and running.

PHY2 Active LED
This LED illuminates when the MediaLB 6-Pin interface of the FPGA is enabled and configured to communicate with an INIC connected to the PHY2 Phy+ Board connector.

PHY2 Phy+ Board Connector
This connector is used to mount a Phy+ Board Variant 1 (optimized for MediaLB 6-Pin communication) to the MITB platform. By default, a Phy+ Board is pre-installed on the MITB platform and the OS81110 on the Phy+ Board has been flashed with the proper firmware.

PHY2 3.3 V Power LED
This LED illuminates when the 3.3 V power supply on the PHY2 Phy+ Board connector has been enabled.

PHY2 MOST Lock LED
This LED illuminates when the OS81110 on the Phy+ Board, which is mounted to the MITB platform, detects MOST Lock.

PHY2 MediaLB Lock LED
This LED illuminates when the OS81110 on the Phy+ Board, which is mounted on the MITB platform, has opened the MediaLB 6-Pin port and the FPGA is locked to the FRAMESYNC signal transmitted by the OS81110.

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3.2 Physical+ Interface Board OS81110 (Phy+ Board)

The Phy+ Board is an add-on-board which can be plugged via a Phy+ Board connector to a main board. It incorporates an OS81110 MOST150 INIC and a Fiber Optic Transceiver (FOT). Connected to the MITB Platform and the user hardware (in case of the MediaLB Device Setup) it is realizing the interface to a MOST150 network.

The delivery of the MITB includes the following Phy+ Boards:

- 1 x Physical+ Interface Board OS81110 (Variant 3)
  - Optimized for MediaLB 3-Pin
  - 47 kΩ pull-down resistors for MediaLB 3-pin signals are assembled
- 2 x Physical+ Interface Board OS81110 (Variant 1)
  - Optimized for MediaLB 6-Pin
  - 100 Ω termination resistors for differential MediaLB 6-pin signal are assembled
  - Pull-down and pull-up resistors required for differential voltage offset on the MediaLB 6-Pin interface are not assembled by default. They need to be available on the main board.

A Phy+ Board Variant 1 is mounted on the MITB platform at delivery. The remaining Phy+ Boards Variant 1 and Variant 3 may be used to realize a MediaLB Device Setup of the MITB as outlined in Figure 2-1: MediaLB Device Setup.

For testing the MediaLB 3-Pin or 6-Pin port of a MDUT, different Phy+ Boards need to be connected to the user hardware:

- MediaLB 3-Pin port testing requires Phy+ Board Variant 3
- MediaLB 6-Pin port testing requires Phy+ Board Variant 1

The layout of the Phy+ Board connector is described in section 3.6.2. For further information on the Physical+ Interface Board including reference schematics, refer to the Physical+ Interface Board OS81110/2+0 Data Sheet [3].

3.3 INIC Explorer Interface Box

The INIC Explorer Interface Box represents the interface between an INIC MOST transceiver and a connected host PC. In combination with the OSS Flasher Software ([7]), the INIC Explorer Interface Box may be used to flash the OS81110 on the MITB Platform or the user hardware. The Interface Box has to be connected to the Customer Configuration Interface of the OS81110 via a 14-bit ribbon cable. An RS232 connection is used to link the Interface Box to the host PC.

For detailed information about the INIC Explorer Interface Box refer to the INIC Explorer User Manual [1].

Hint The INIC Explorer Interface Box is not delivered with the MITB. It has to be purchases separately [1].

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3.4 MediaLB Analyzer

The MediaLB Analyzer is a tool designed to observe and visualize MediaLB data in a comfortable way. It consists of the following hardware and software modules:

Hardware Modules

- MediaLB Monitor USB – converter box transferring MediaLB data received from Active-Pods via USB 2.0 to a host PC
- Active-Pods – functioning as interface to the MediaLB port of the Device Under Test

Software Module

- OptoLyzer Suite – software, which supports analysis and visualization of MediaLB data

Hint The components of the MediaLB Analyzer need to be purchased separately to complete a MediaLB Analyzer setup.
Active-Pods have to be purchased dependent on the MediaLB interface (3-Pin or 6-Pin) to be analyzed and the used MediaLB debug header (low-speed or high-speed).

A typical MITB setup comprises only MediaLB 3/6-Pin high-speed debug headers. Therefore, it is recommended to purchase 3-Pin and/or 6-Pin high-speed Active-Pods for usage on the MITB.

For further information on the MediaLB Analyzer refer to the MediaLB Analyzer User Manual [2].

3.5 Host PC

The host PC should be a standard Pentium class PC or laptop on which the GUI of the MITB and the OSS Flasher Software [7] need to be installed.

The minimum requirements for the host PC are outlined in section 2.4.

The host PC has to be connected to the MITB Platform as well as the INIC Explorer Interface Box by an RS232 connection. If RS232 to USB converters are used, the INIC Explorer Interface Box and the MITB platform may be connected via USB to the host PC.

3.6 Connectors

Four kinds of connectors are available on a MITB setup:

- Configuration/debug header
- Phy+ Board connector
- MediaLB 3/6-Pin high-speed debug header
- Trigger connector

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The configuration/debug header is required to flash the firmware or to modify the configuration string of an OS81110 MOST transceiver.

The Phy+ Board connector is used to connect a Phy+ Board to a main board (e.g., MITB platform or to user hardware). The MediaLB 3/6-Pin high-speed debug header is suitable to connect a MediaLB Analyzer for observation and debugging the data flow on a MediaLB interface.

The Phy+ Board connector and the MediaLB 3/6-Pin high-speed debug header are physically identical. Both headers are high-speed differential connectors with 40 pins or 20 differential pairs. The difference between both connectors is the signal layout.

The Phy+ Board connector incorporates all interface signals of the OS81110 INIC including MediaLB 3/6-Pin, I^2S, SPI, TSI, I^2C and JTAG. The MediaLB debug connector comprises the MediaLB 3-Pin and 6-Pin signals only.

For every MediaLB data type, the trigger connector features a pin used to generate events in case the PGA detects error conditions.

A detailed layout of the connectors is shown in the following sections.

3.6.1 Configuration/Debug Header

For proper operation of the MITB a dedicated test firmware needs to be flashed to the OS81110 connected to the MDUT. The configuration/debug header is defined to flash the OS81110 via its JTAG Port. With SMSC's INIC Explorer tool, which can be directly connected to the configuration/debug header, the OS81110 on a Phy+ Board or on the user hardware can be flashed.

The configuration/debug header is defined as a standard 14-Pin (2 x 7) 2 mm header (such as Molex 87332-1420 or equivalent).

The following figure outlines the configuration/debug header including the connection to the OS81110 INIC. For further details please refer to the OS81110 Data Sheet [5].

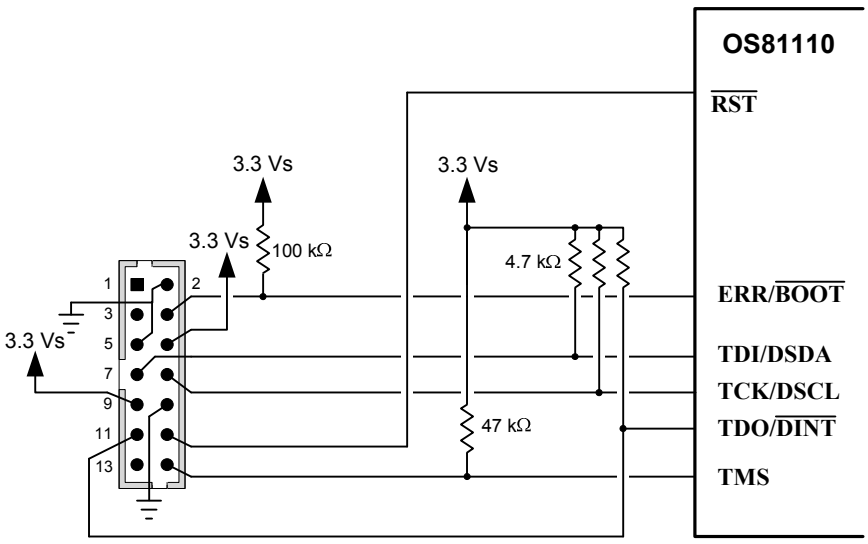

Figure 3-2: Configuration Debug Header

3.6.2 Phy+ Board Connector

To connect a Phy+ Board to a main board a Phy+ Board connector is used.

An example Phy+ Board connector is:
SAMTEC 0.5 mm, 20-pair, high-speed differential pair socket QSH-020-01-L-D-DP-A

The layout of the Phy+ Board connector is outlined below. For more detailed information please refer to the Physical+ Interface Board OS81110 Data Sheet [3].

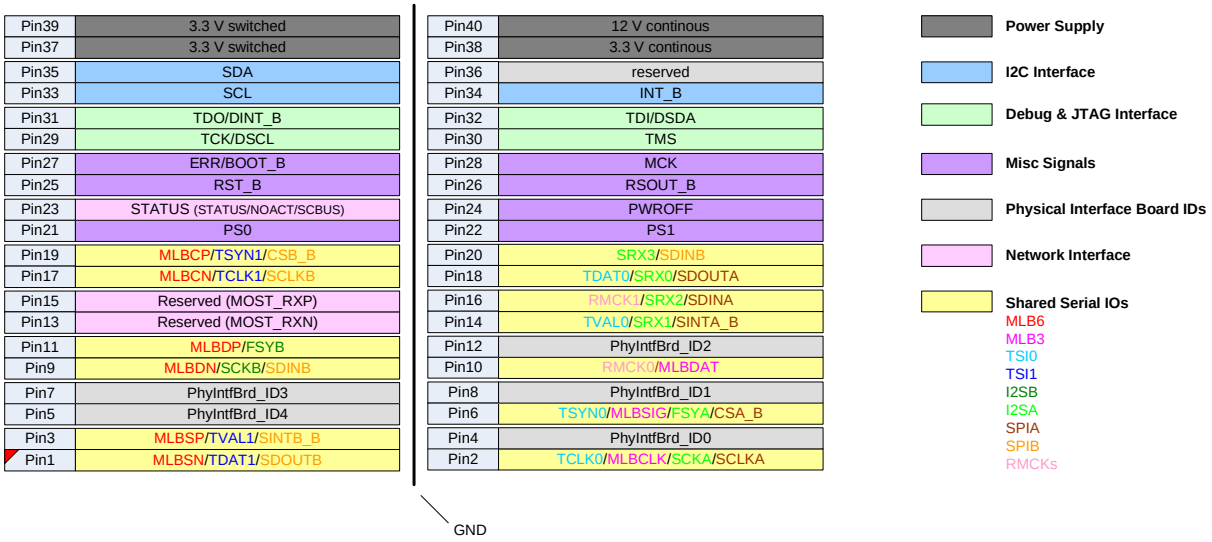

Figure 3-3: Phy+ Board Connector

The Phy+ Board connector needs to be available on the user hardware if the MITB is configured as MediaLB Device Setup. In this case, a Phy+ Board must be connected to the user hardware to complete the setup (see paragraph 3.6.2.1 for detailed description) For a MOST150 Device Setup no Phy+ Board connector is required on the user hardware, because the functionality of the Phy+ Board is an integral part of the user hardware.

3.6.2.1 Wiring of Phy+ Board Connector for MediaLB Device Setup

To connect the Phy+ Board to the user hardware in the MediaLB Device Setup the following general information and instructions on wiring and termination need to be followed:

- In case of OS81050 and OS81110 Phy Board 12 V supply is not required. In case of OS81082/92 PhyBoard 12 V is required.
- If no power management is required the 3.3 V switched and 3.3 V continuous supply can be tied together from a single supply.
- If I2C is not used no termination is required on I2C signals. But if possible it is recommended to connect the I2C interface. Possible use cases are flashing of INIC firmware via EHC or initial communication with INIC for debug purposes.
- The ID pins are configured on the PHY Boards. They may be used on the user boards to identify the PHY Boards connected. The definition of the ID signals can be found in the datasheets of the PHY Boards. If the ID pins are evaluated on the user board pull-ups are required. If the ID pins are unused no termination is required.
- MISC signals do not require termination and may be unconnected.
- Signals that are not planned to be used like I2C above (serial I2S and Transport stream interfaces) do not require termination and may be unconnected.

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- For testing the MediaLB 3-pin interface of the DUT OS81110 Phy+ Boards Variant 3 need to be used. On these Phy+ Boards, 47 KOhm pull-down resistors as well as 47 Ohm series resistors close to the INIC are present on all MediaLB 3-pin signals (see the schematic in the Phy+ Board data sheet for details). It is recommended to implement series termination resistors as close as possible to the DUT/MediaLB Device as outlined in the MediaLB Specification ([4]) Figure 2-1. And optionally also a RC termination on the MLBCLK line may be implemented to provide the possibility to improve signal integrity if required. Please note, that the resistors and capacitors values shown in the MediaLB Specification are recommendations only. Values chosen in actual systems are based on the MediaLB clock speed, impedance of the PCB traces, and the load capacitance on the line.
- For testing the MediaLB 6-pin interface of the DUT OS81110 Phy+ Boards Variant 1 need to be used. On these Phy+ Boards, 100 Ohm termination resistors are present on all differential MediaLB 6-pin signals close to the INIC. Pull-up and pull-down resistors as defined in the MediaLB Specification (see [4] Figure 2-6 for details) are not assembled by default, but there are place holders prepared to assemble the required pull-up and pull-down resistors on the MLBSP/N and MLBDP/N signals. For details about calculation of required pull-up and pull-down resistors refer to MediaLB Specification V4.2 ([4]) section A.3.2. Please note, that the resistors and capacitors values shown in the MediaLB spec are recommendations only. Values chosen in actual systems are based on the MediaLB clock speed, impedance of the PCB traces, and the load capacitance on the line.
- PWROFF signal is an output from INIC and may be connected to input of EHC.
- Apart from the MLB signals, the following signals are recommended to be connected on the user board:
    - RST_B - power on reset through a 0ohm resistor to the reset of user board
    - SCL, SDA, INT_B - to GPIOs on EHC
    - PWROFF - to GPIO on EHC
    - RMCK1 - optionally to an external reference clock (through 0 ohm).
- Except of the MediaLB 6-pin signals on the user board no termination circuit is required.
- The MediaLB 3-pin signal levels are dependant of the INIC on the Phy+ Boards. For detailed information refer to the INIC data sheets. On OS81110 the MediaLB 3-pin signal levels are of type 3.3V and on OS81050 the levels are of type 2.5V.

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3.6.3 MediaLB 3/6-Pin High-Speed Debug Header

The MediaLB 3/6-Pin high-speed debug header represents a differential high-speed connector used to connect a MediaLB Analyzer for observation of data transfer on a MediaLB interface. Especially for MediaLB 6-Pin debugging it is essential that this 40-pin header can support high-speed data rates.

An example header is:
SAMTEC 0.5 mm, 20 pair, high-speed, differential pair socket QSH-020-01-L-D-DP-A

For more details including schematic and PCB layout recommendations refer to the MediaLB Specification [4].

The MediaLB debug header is physically identical to the Phy+ Board connector but as outlined in Figure 3-4: MediaLB 3/6-Pin High-Speed Debug Header the MediaLB debug header incorporates only the MediaLB 3-Pin and 6-Pin signals as a subset of the available signal on the Phy+ Board connector.

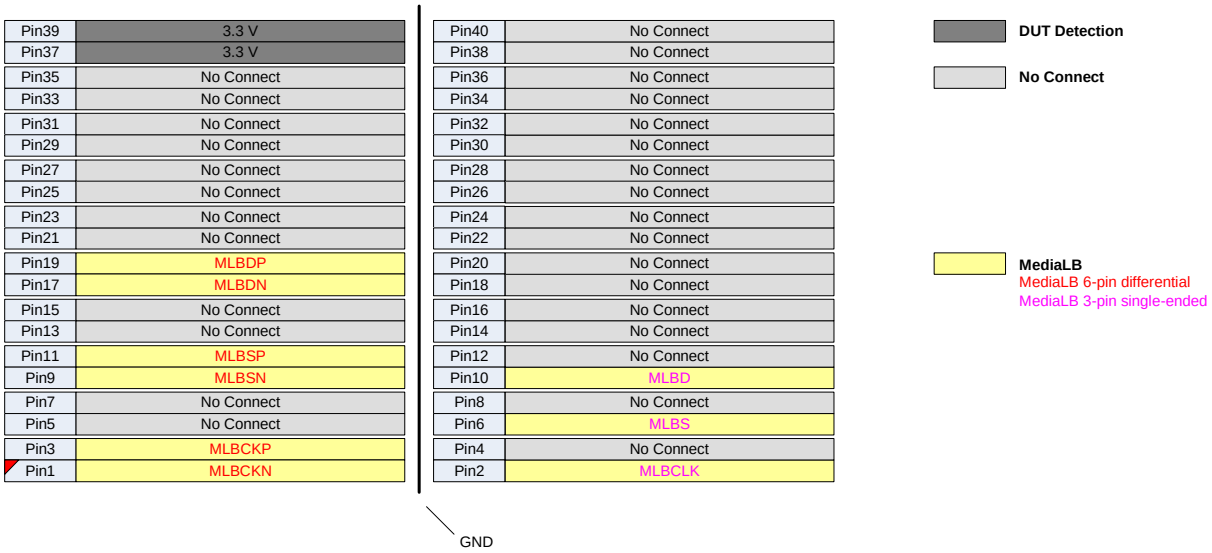

Figure 3-4: MediaLB 3/6-Pin High-Speed Debug Header

At a MOST150 Device Setup the MediaLB debug header needs to be available on the user hardware to enable the connection of a MediaLB Analyzer. If the MITB is used in MediaLB Device Setup, the MediaLB debug header does not need to be available on the user hardware, because a MediaLB Analyzer can be directly connected to the Phy+ Board plugged on the user hardware.

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3.6.4 Trigger Connector

The trigger connector is available on the MITB platform. It features four trigger output signals. For every MediaLB data type, the PGA is asserting one of the trigger signals in case an error is detected in the received data stream. Connected to either an oscilloscope or the high-speed trigger input of a MediaLB Analyzer, the trigger signals can be used to capture error conditions.

Pin1	No connect
Pin3	Control Trigger Output
Pin5	Sync Trigger Output
Pin7	No connect
Pin9	No connect
Pin11	No connect
Pin13	No connect
Pin15	No connect
Pin17	No connect
Pin19	No connect
Pin21	No connect
Pin23	No connect
Pin25	No connect
Pin27	No connect
Pin29	No connect
Pin31	No connect
Pin33	No connect
Pin35	No connect
Pin37	GND
Pin39	GND
Pin41	12 V Input
Pin43	GND
Pin45	5 V
Pin47	GND
Pin49	3.3 V

Pin2	No connect
Pin4	Async Trigger Output
Pin6	Isoc Trigger Output
Pin8	No connect
Pin10	No connect
Pin12	No connect
Pin14	No connect
Pin16	No connect
Pin18	No connect
Pin20	No connect
Pin22	No connect
Pin24	No connect
Pin26	No connect
Pin28	No connect
Pin30	No connect
Pin32	No connect
Pin34	No connect
Pin36	No connect
Pin38	GND
Pin40	GND
Pin42	12 V Input
Pin44	GND
Pin46	5 V
Pin48	GND
Pin50	3.3 V

Trigger Output Signals

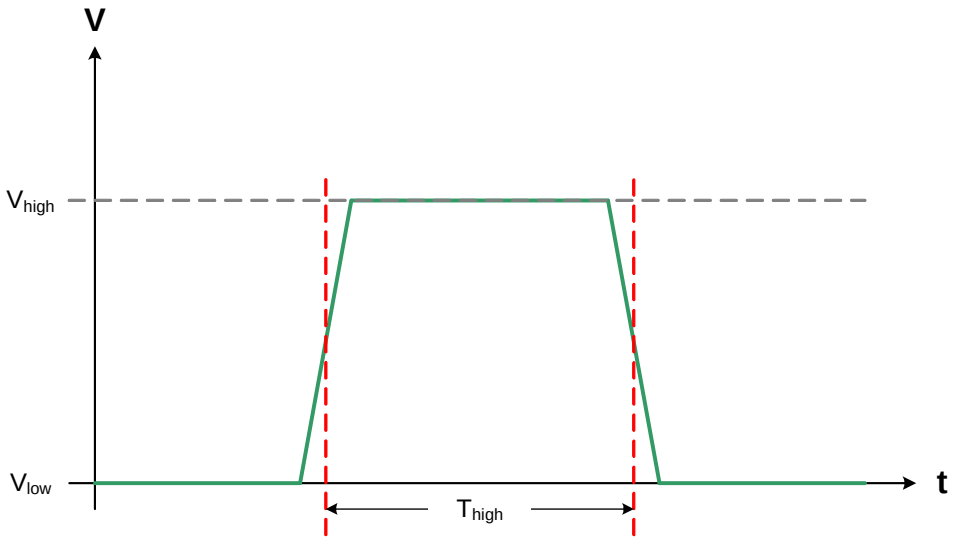
No connect

GND

Power Supply
There is no need to use these signals!

Figure 3-5: Trigger Connector

The shape of the generated trigger events are shown in the following figure.



V_{high} = 3.3 V

V_{low} = 0 V

T_{high} = 2..12 µs

Figure 3-6: Trigger Event

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3.7 MediaLB Device Under Test

The MDUT represents a MediaLB device implemented by the user. The functional capabilities of the MDUT depend on the user-specific device implementation. While some devices may support all kind of MediaLB parameters such as different clock speeds (256xFs, 512xFs…), interface modes (3-Pin and 6-Pin) or data transfer types (control, asynchronous, synchronous and isochronous) other devices may support only a sub-set of the possible MediaLB functionality.

The MITB provides test cases for a wide variety of MediaLB parameters. Dependent on the functionality supported by the MDUT, the user can decide which of the provided test cases are useful to be tested at its MediaLB device. The test cases defined by the MITB are described in chapter 7.

3.7.1 Loop-Back Functionality

The loop-back functionality on the MediaLB Device Under Test is a precondition for correct operation of test cases and required to perform the test scenarios provided by the MITB. The loop-back functionality includes the capability to receive data patterns on a MediaLB Rx channel and re-transmit the patterns on a Tx channel without modifying the patterns.

The transferred test patterns are generated by the PGA part of the MITB and are transmitted on a Tx channel of the MediaLB Controller connected to the MDUT. The patterns re-transmitted by the MDUT are received by the MediaLB controller and analyzed by the PGA. Errors in the received pattern are reported on the GUI of the MITB.

The test patterns can be of any data type such as control, asynchronous, synchronous or isochronous data. The MITB comprises test cases transferring single data types as well as combined test cases with the concurrent transfer of several data types.

The test definitions include ChannelAddresses used to transmit and receive test patterns. To successfully run a selected test, the MDUT must be configured to receive and re-transmit the patterns generated by the MITB on the defined MediaLB ChannelAddresses. Additionally, the MDUT must be configured for the correct interface mode (3-Pin or 6-Pin), clock speed (256xFs, 512xFs…) and data type (control, asynchronous, synchronous or isochronous data).

The following figure shows an example how the loop-back functionality works. The MDUT receives data from MediaLB on ChannelAddress 0x0002 and re-transmits the received pattern on ChannelAddress 0x0004.

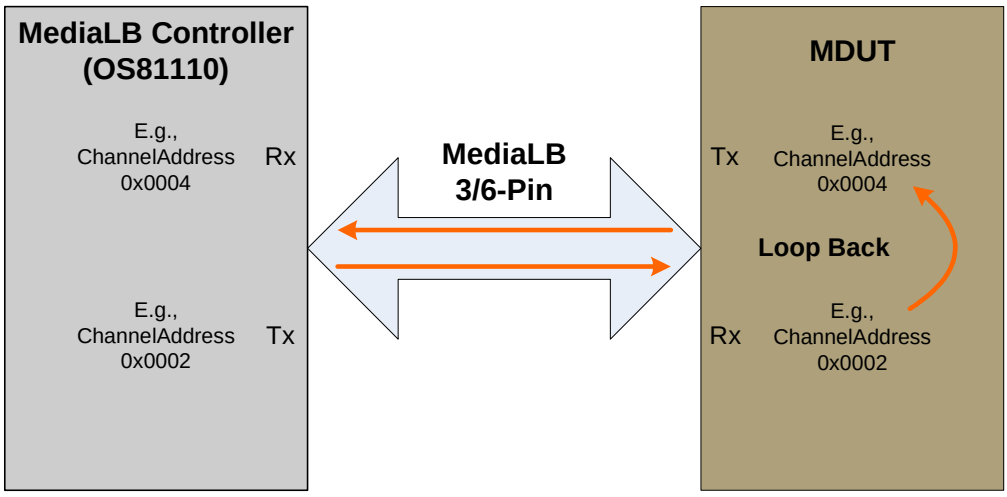

Figure 3-7: Loop-Back

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4 Set-Up the Test Bench

In sections 2.1.1 and 2.1.2 of this user manual the MediaLB Device Setup and the MOST150 Device Setup of the MITB are described. It is up to the user to establish the mandatory connections displayed in Figure 2-1: MediaLB Device Setup and Figure 2-2: MOST150 Device Setup to realize the most suitable setup for MediaLB device testing.

4.1 Connect MITB Platform to Host PC

The MITB platform has to be connected to a host PC or laptop via an RS232 cable. The RS232 cable is provided with the package of the MITB. To establish the connection the lower RS232 port of the MITB platform (see section 3.1 for details) needs to be linked to a free RS232 port on the host PC.

4.2 Connect MITB Platform to User Hardware

The MITB platform and the user hardware have to be connected via an optical MOST150 network using the two optical fiber cables with Yazaki 2+0 connectors. The two boards have to be connected in a way, that the fibers form an optical loop.

4.3 Connect INIC Explorer Interface Box

The INIC Explorer Interface Box needs to be connected to the configuration/debug header on the Phy+ Boards or the user hardware via a 14-pin ribbon cable delivered with the INIC Explorer Interface Box. In addition, the box has to be linked via an RS232 cable to a free port of the host PC.

For detailed information on the INIC Explorer refer to the INIC Explorer User Manual [1].

4.4 Connect MediaLB Analyzer

For connecting the MediaLB Analyzer refer to the MediaLB Analyzer User Manual [2].

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5 Flashing the MITB Platform

FPGA images as well as Pattern Generator & Analyzer firmware can be flashed to the MITB platform. To perform the flashing, the MITB platform needs to be connected to a host PC or laptop via Ethernet. An Ethernet crossover cable is part of the MITB delivery and used to link a host PC to the RJ-45 Ethernet connector of the MITB platform (see section 3.1 for details).

A PCFlasher application needs to be executed on the host PC to enable flashing. The PCFlasher is available on the Installation CD of the MITB package.

To initiate a flash process, the user buttons described in section 3.1 need to be pressed.

The following figure shows the connection of the MITB platform and a host PC.

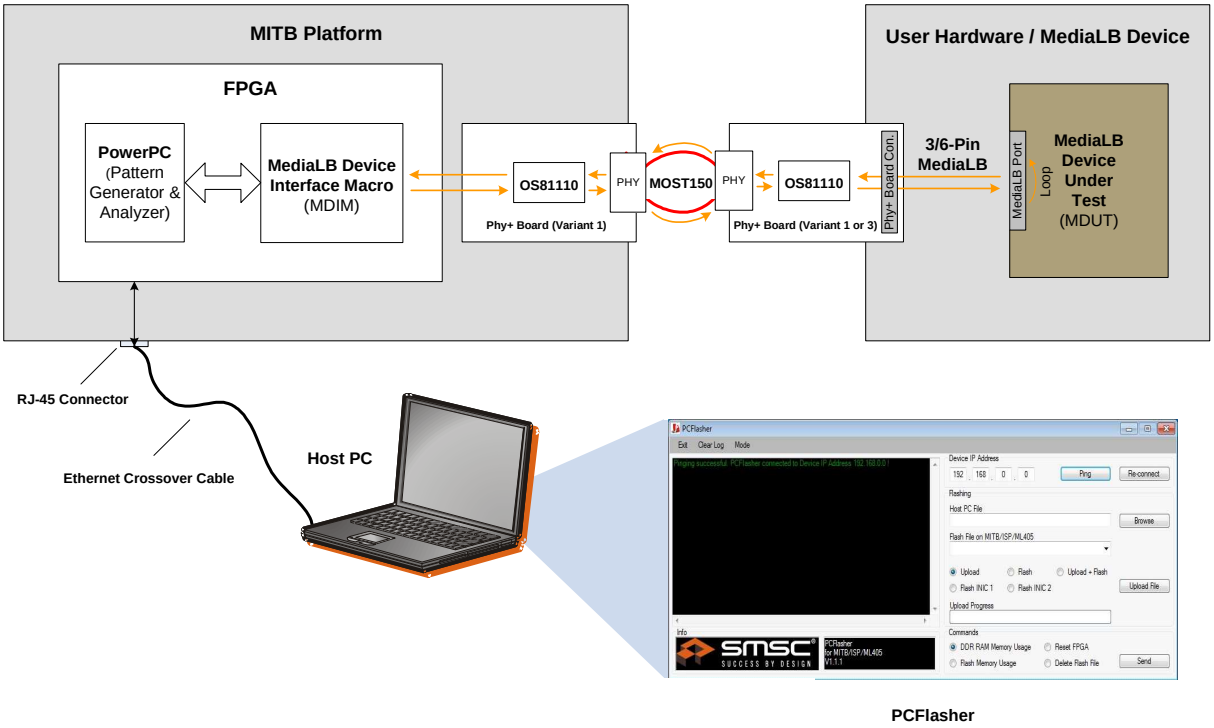

Figure 5-1: Ethernet Connection MITB Platform and Host PC

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5.1 Setup IP Address on Host PC

The MITB platform is configured for IP address ***192.168.0.100***.

To enable proper communication between the MITB platform and the connected host PC, the IP address on the PC needs to be set to ***192.168.0.1*** as shown in the following figure.

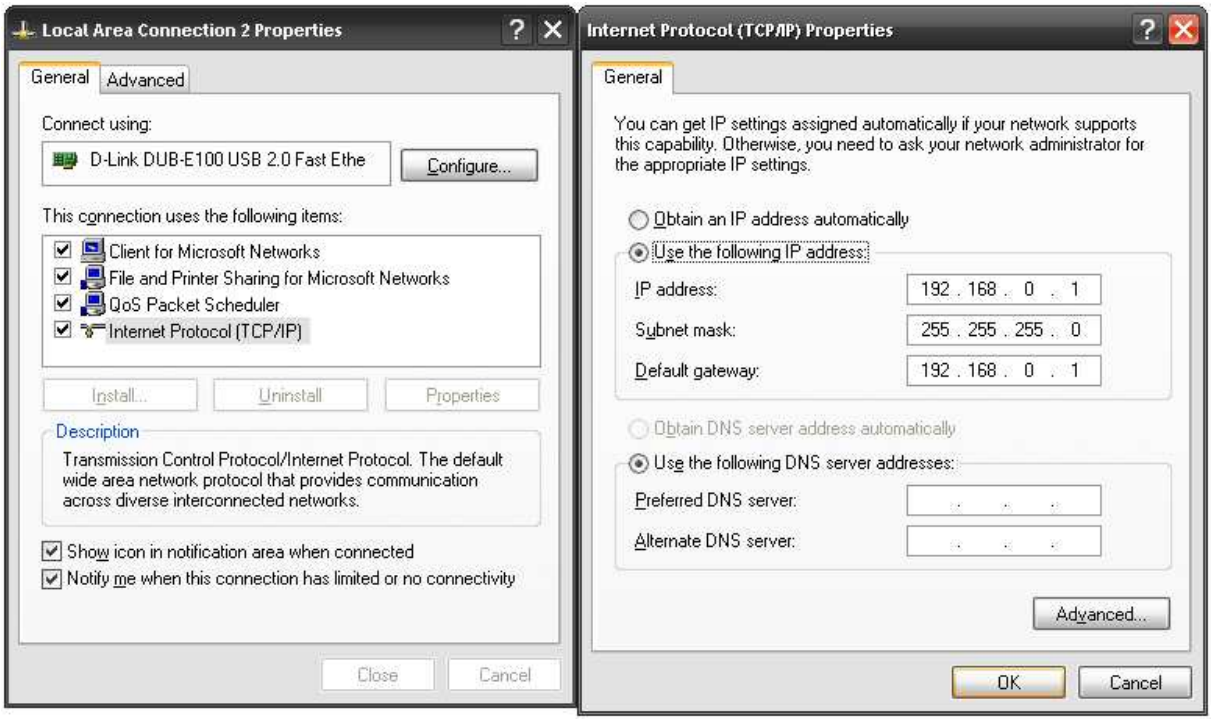
Local Area Connection 2 Properties
General
Advanced
Connect using:
D-Link DUB-E100 USB 2.0 Fast Ethe
Configure...
This connection uses the following items:
Client for Microsoft Networks
File and Printer Sharing for Microsoft Networks
QoS Packet Scheduler
Internet Protocol (TCP/IP)
Install...
Uninstall
Properties
Description
Transmission Control Protocol/Internet Protocol. The default wide area network protocol that provides communication across diverse interconnected networks.
Show icon in notification area when connected
Notify me when this connection has limited or no connectivity
Close
Cancel
Internet Protocol (TCP/IP) Properties
General
You can get IP settings assigned automatically if your network supports this capability. Otherwise, you need to ask your network administrator for the appropriate IP settings.
Obtain an IP address automatically
Use the following IP address:
IP address: 192 . 168 . 0 . 1
Subnet mask: 255 . 255 . 255 . 0
Default gateway: 192 . 168 . 0 . 1
Obtain DNS server address automatically
Use the following DNS server addresses:
Preferred DNS server:
Alternate DNS server:
Advanced...
OK
Cancel

Figure 5-2: IP Address Configuration on Host PC

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5.2 Flash FPGA Image

To flash an FPGA image to the MITB platform the following steps are required:

1. Power-up MITB platform:
   - Power-up MITB platform while user button ***WEST*** is pressed.
   - Button needs to be pressed for several seconds until Flashloader application will be executed on the MITB platform.
   - The version of the Flashloader is indicated on the LCD display next to the user buttons.

2. Run PCFlasher.exe:
   - Start PCFlasher.exe application on host PC (the PCFlasher.exe file is provided on the CD delivered with the MITB platform).

3. Verify connection to MITB platform:
   - The IP address of MITB platforms is defined as: ***192.168.0.100***.
   - Enter IP address of MITB platform in the GUI of the PCFlasher application.
   - Click the ***Ping*** button.
   - Connection success is reported by the log window.

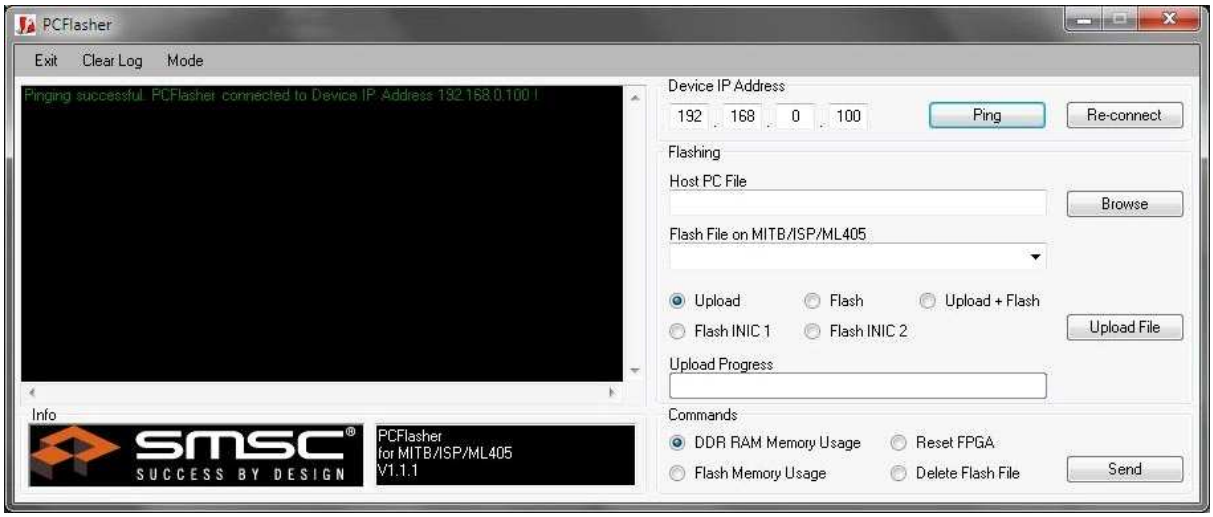

Figure 5-3: Verify Connection to MITB Platform

4. Load FPGA image file to MITB platform:
   - Open the ***Browse*** dialog and select the FPGA image to be flashed (e.g. ***SP89420_vhdl_v02_02_13-01_bootloader_v00_05_08-01.xsvf***).
   - The FPGA image needs to be available in xsvf format.
   - The selected file name must have less than 63 characters.
   - Configure PCFlasher to ***PowerPC Application*** via the ***Mode*** menu.
   - Select the ***Upload*** check box and click ***Upload File*** button.
   - The log window indicates if the selected file has been properly loaded to the MITB platform.

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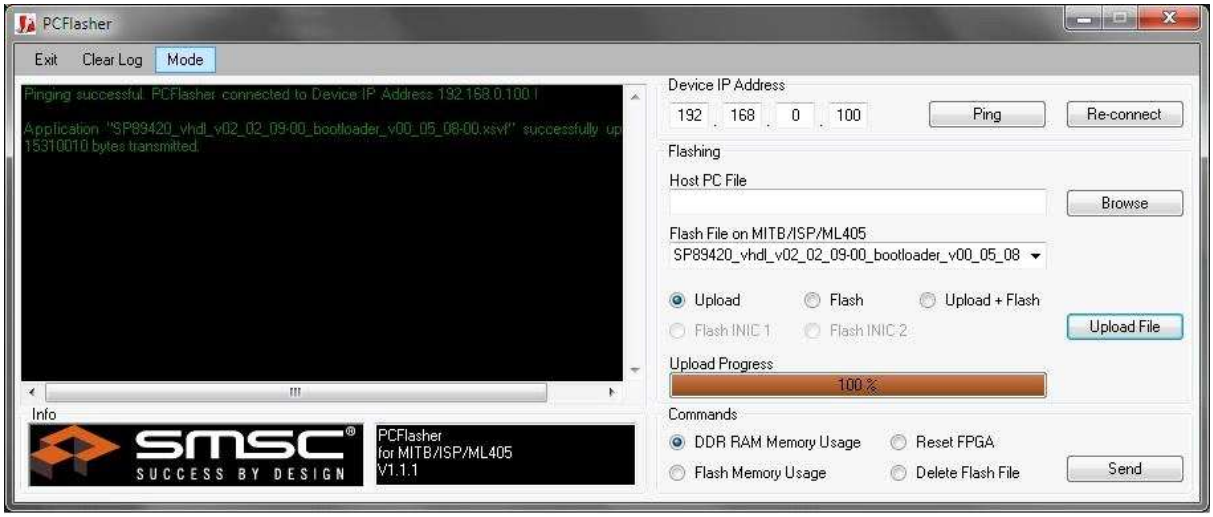

Figure 5-4: Load FPGA Image File to MITB Platform

5. Flash FPGA image to MITB platform:
   - Select the ***Flash*** check box and click the ***Flash Board*** button.

Note Do not interrupt the flash process!
Flashing of FPGA image can take up to five minutes.

- The log window indicates if the selected file has been properly flashed.

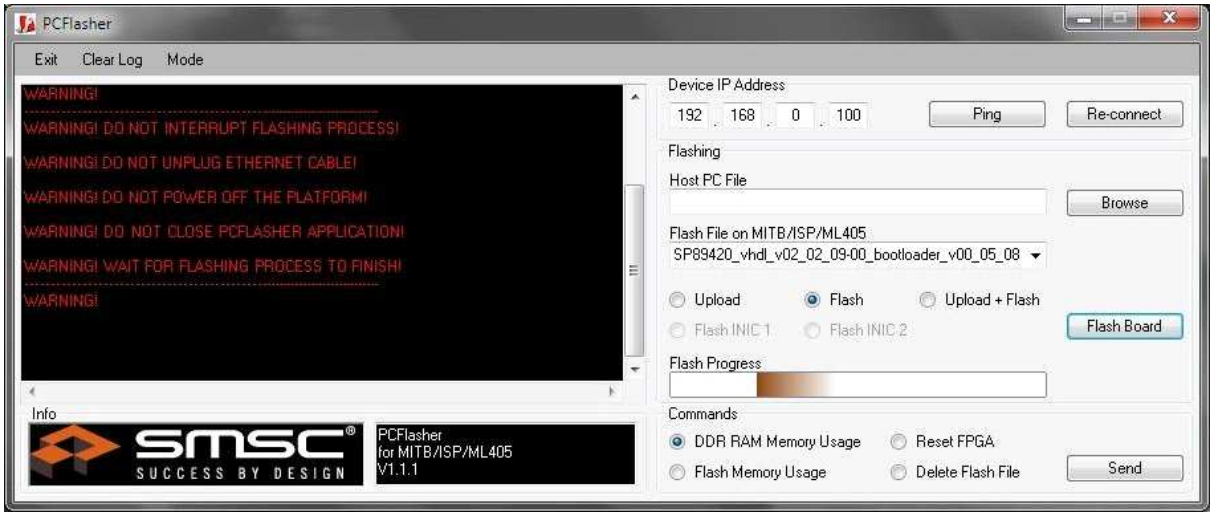

Figure 5-5: Flash FPGA Image to MITB Platform

6. Load FPGA image:
   - Power-up MITB platform.
   - Do not press any button!
   - New image will be loaded to FPGA.
   - For a few seconds, the version of the FPGA image is indicated on the LCD display (next to the user buttons).

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5.3 Flash Pattern Generator & Analyzer

To flash Pattern Generator & Analyzer firmware to the MITB platform, the following steps are required:

1. Power-up MITB platform:
   - Power-up the MITB platform while user button ***WEST*** is pressed.
   - Button needs to be pressed for several seconds until Flashloader application will be executed on the MITB platform.
   - The version of the Flashloader is indicated on the LCD display next to the user buttons.

2. Run PCFlasher.exe:
   - Start PCFlasher.exe application on host PC (the PCFlasher.exe file is provided on the CD delivered with the MITB platform).

3. Verify connection to MITB platform:
   - The IP address of MITB platforms is defined as: ***192.168.0.100***.
   - Enter IP address of MITB platform in the GUI of the PCFlasher application.
   - Click the ***Ping*** button.
   - In the log window connection success should be reported.

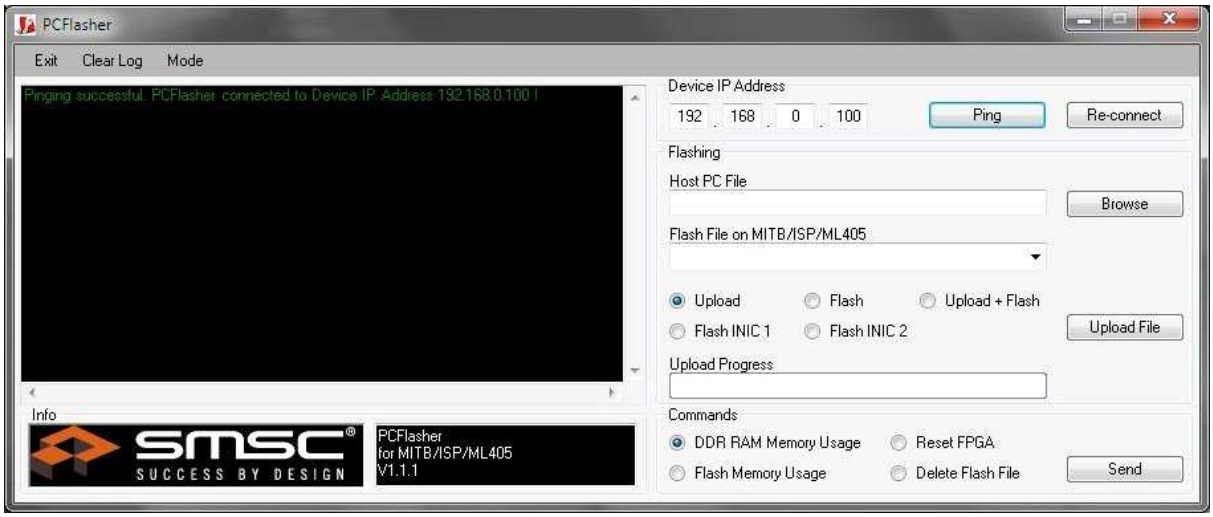

Figure 5-6: Verify Connection to MITB Platform

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4. Load Pattern Generator & Analyzer firmware file to MITB platform:
   - Open the ***Browse*** dialog and select the file to be flashed (e.g. ***MITB_PGA_V02_02_00-01.srec***).
   - The firmware file needs to be available in srec format.
   - The selected file name must have less than 63 characters.
   - Configure PCFlasher to ***PowerPC Application*** via the ***Mode*** menu.
   - Select the ***Upload*** check box and click the ***Upload File*** button.
   - The log window indicates if the selected file has been properly loaded to the MITB platform.

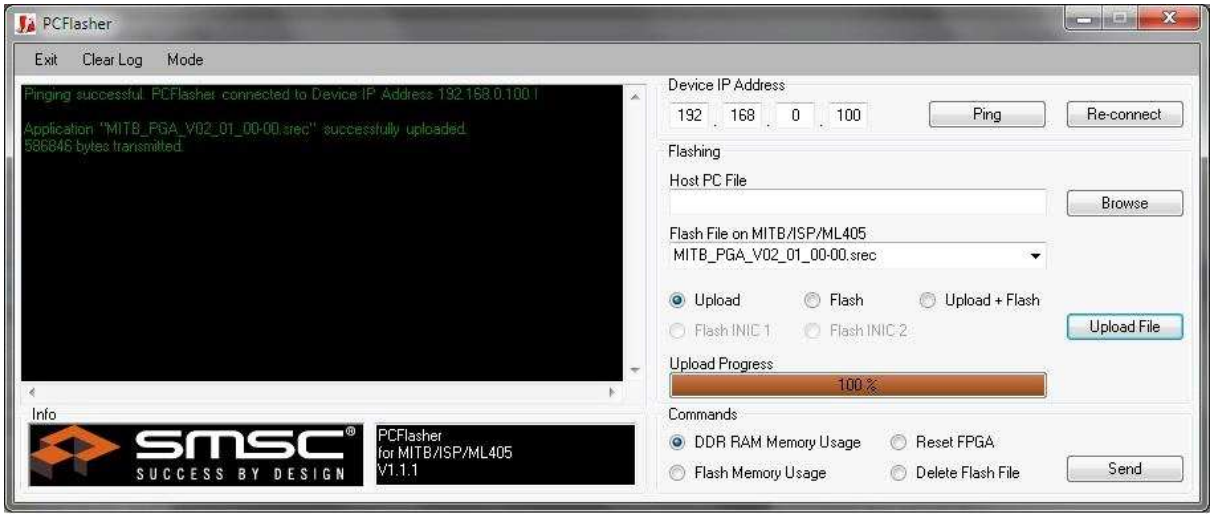

Figure 5-7: Load Pattern Generator & Analyzer Firmware to MITB Platform

5. Flash Pattern Generator & Analyzer firmware MITB Platform:
   - Select the ***Flash*** check box and click the ***Flash Board*** button.

Note Do not interrupt flash process!
Flashing of the firmware will take several seconds.

- The log window indicates if the selected file has been properly flashed.

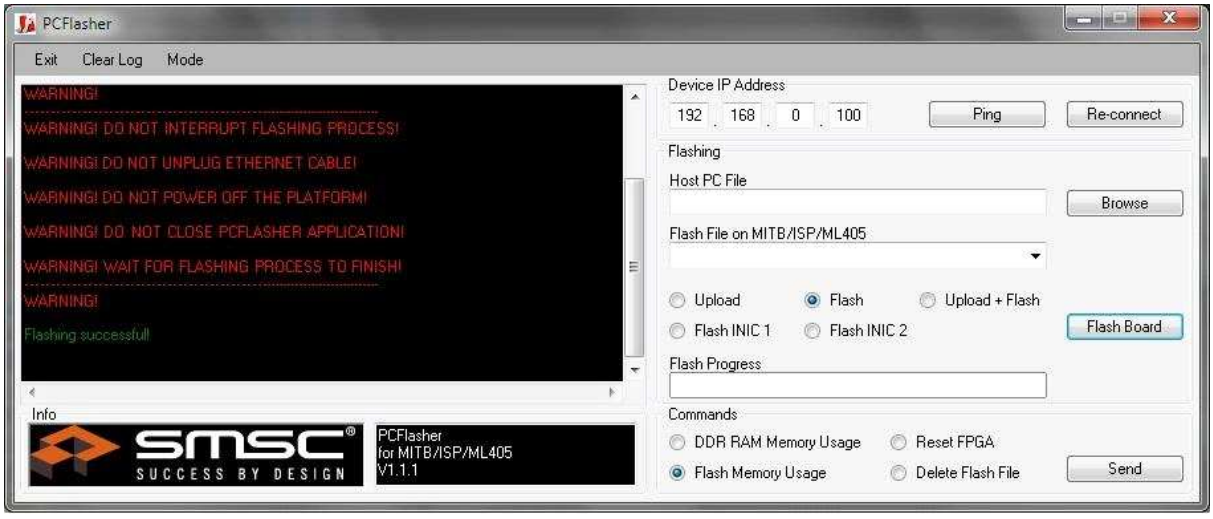

Figure 5-8: Flash Pattern Generator & Analyzer to MITB Platform

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6. Run Pattern Generator & Analyzer:
   - Power-up MITB platform.
   - Do not press any button!
   - Flashed Pattern Generator & Analyzer will be loaded.
   - The version of the flashed Pattern Generator & Analyzer is indicated on the LCD display next to the user buttons.

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6 Configure the Test Bench

To verify the proper implementation of an MDUT, it is required to configure the MITB and the generated test patterns. The MITB configuration includes the setup of the PGA as well as the configuration of the OS81110 devices part of the MITB setup. The configuration of the MITB can be done by means of a GUI, which is running on the host PC.

6.1 Execute the Graphical User Interface

The MITB GUI runs on a host PC or laptop with a Windows OS (XP or 2000) and supports communication with the MITB via an RS232 interface. The GUI is part of the MITB delivery and can be found on the installation CD. For details about the files provided on the installation CD refer to chapter 9, Summary of Provided Files.

To start the GUI double click the provided *MITB_GUI_V02_02_XX.exe* file.

Parameters entered by the user on the GUI are saved to the file *MITB_GUI_Parameters.ini* when the GUI is closed and re-loaded, when the GUI is started again.

6.2 Description of the Graphical User Interface

The following figure depicts the main window of the GUI.

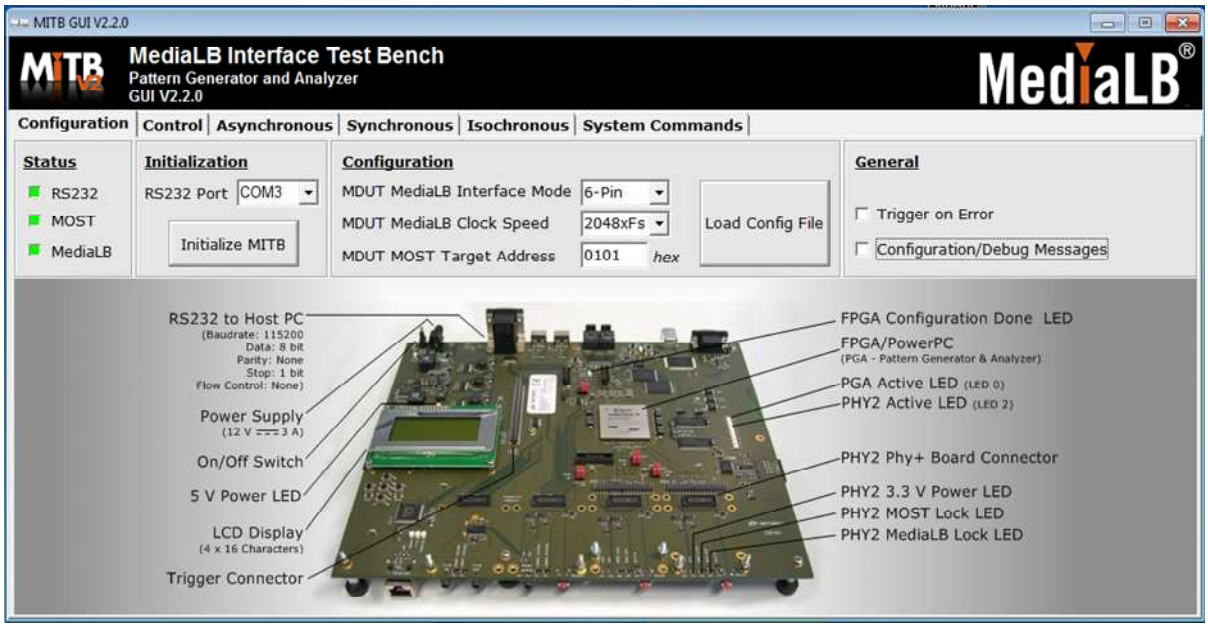

Figure 6-1: GUI – Main Window

The GUI features several tabs, including:

- **Configuration tab**: Defines general configuration parameters
- **Control tab**: Defines parameters for control message tests
- **Asynchronous tab**: Defines parameters for asynchronous packet tests
- **Synchronous tab**: Defines parameters for synchronous streaming data tests
- **Isochronous tab**: Defines parameters for isochronous data tests
- **System Commands tab**: Defines parameters to generate system commands

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6.2.1 Configuration Tab

The following figure shows the configuration tab of the GUI.

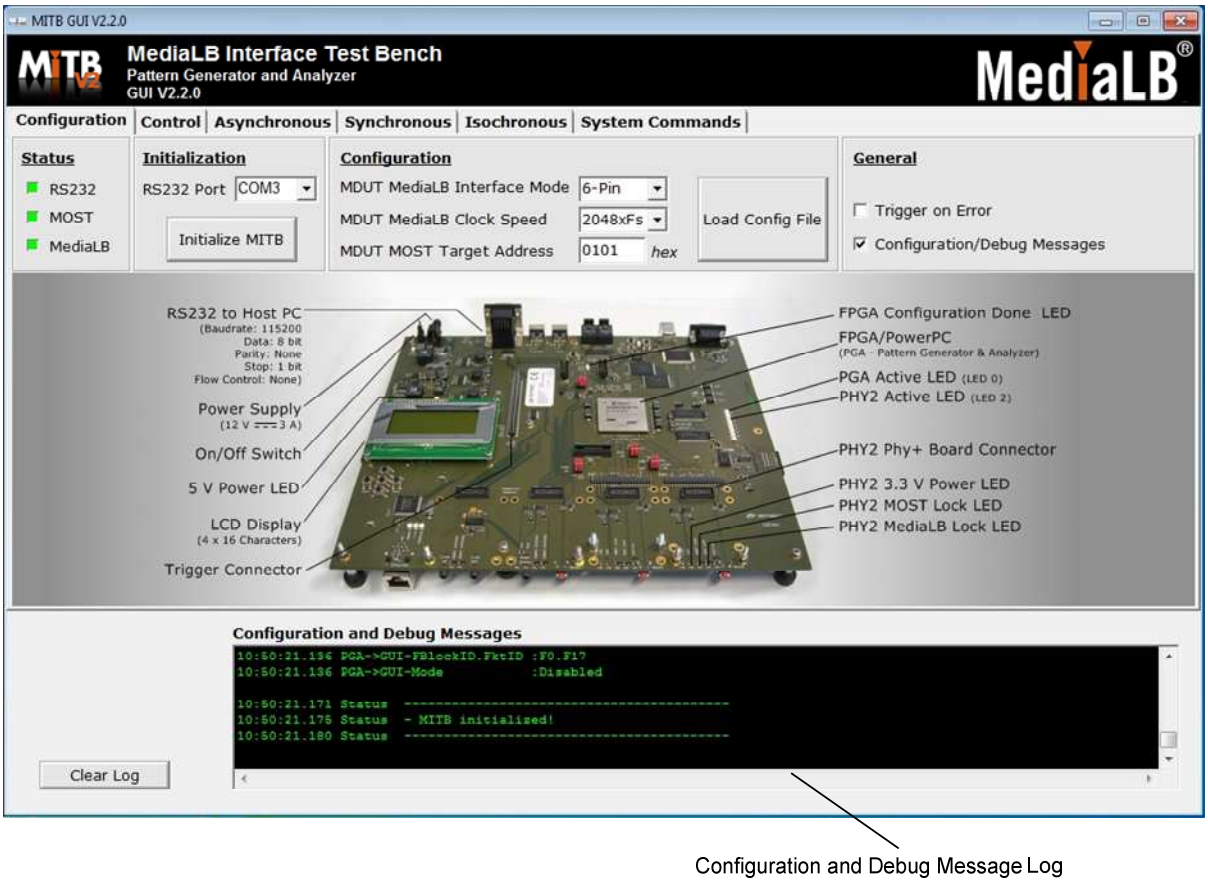

Figure 6-2: Configuration Tab

6.2.1.1 Configuration Tab Parameters

Indicators, buttons and parameters of the configuration tab are described in the table below.

Name	Description
Status	
RS232	Red: RS232 connection to MITB not available Yellow: RS232 connection to MITB in progress Green: RS232 connection to MITB established
MOST	Red: MOST Unlock – Network connection between MITB and MDUT not available Yellow: MOST Network configuration in progress Green: MOST Lock – Network connection between MITB and MDUT established
MediaLB	Red: MediaLB Unlock – PGA not locked to MediaLB Yellow: MediaLB configuration in progress Green: MediaLB Lock – PGA locked to MediaLB

Table 6-1: Configuration Tab Parameters (Part 1)

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Name	Description
Initialization	
RS232 Port	Serial COM port of the host PC used for RS232 communication with MITB platform
Initialize MITB	Button used to initialize MITB with the parameters entered on the Configuration tab
Configuration	
MDUT MediaLB Interface Mode	Defines the MediaLB interface mode (3-Pin or 6-Pin) of the OS81110 connected to the MDUT
MDUT MediaLB Clock Speed	Defines the MediaLB clock speed (256xFs, 512xFs…) of the OS81110 connected to the MDUT
MDUT MOST Target Address	Defines the MOST target address of the OS81110 connected to the MDUT
Load Config File	Button to load test configuration files
General	
Trigger on Error	Check box used to enable/disable the generation of events on the trigger connector in case of detected errors. Check box is valid for all data types.
Configuration/Debug Messages	Check box used to enable/disable the visibility of a debug window showing the communication between GUI, PGA and the INIC on the user hardware.

Table 6-2: Configuration Tab Parameters (Part 2)

6.2.1.2 Configuration and Debug Messages Log

The visibility of the Configuration and Debug Messages Log can be enabled and disabled by the Configuration/Debug Messages check box on the configuration tab of the GUI. The log window displays the messages transferred between the GUI and the PGA as well as the messages exchanged between the GUI and the INIC connected to the MDUT. Additionally, status information is provided about the state of the MITB initialization and the pattern generation.

The Configuration and Debug Messages Log can be cleared by clicking the “Clear Log” button located next to the log window.

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6.2.2 Control Tab

The following figure shows the control tab of the GUI. In this tab parameters can be entered, which define the characteristics of the generated control test patterns. A button is available to manually start and stop the pattern processing. Log windows display the PGA results and statistics. Dedicated test status fields indicate the test status.

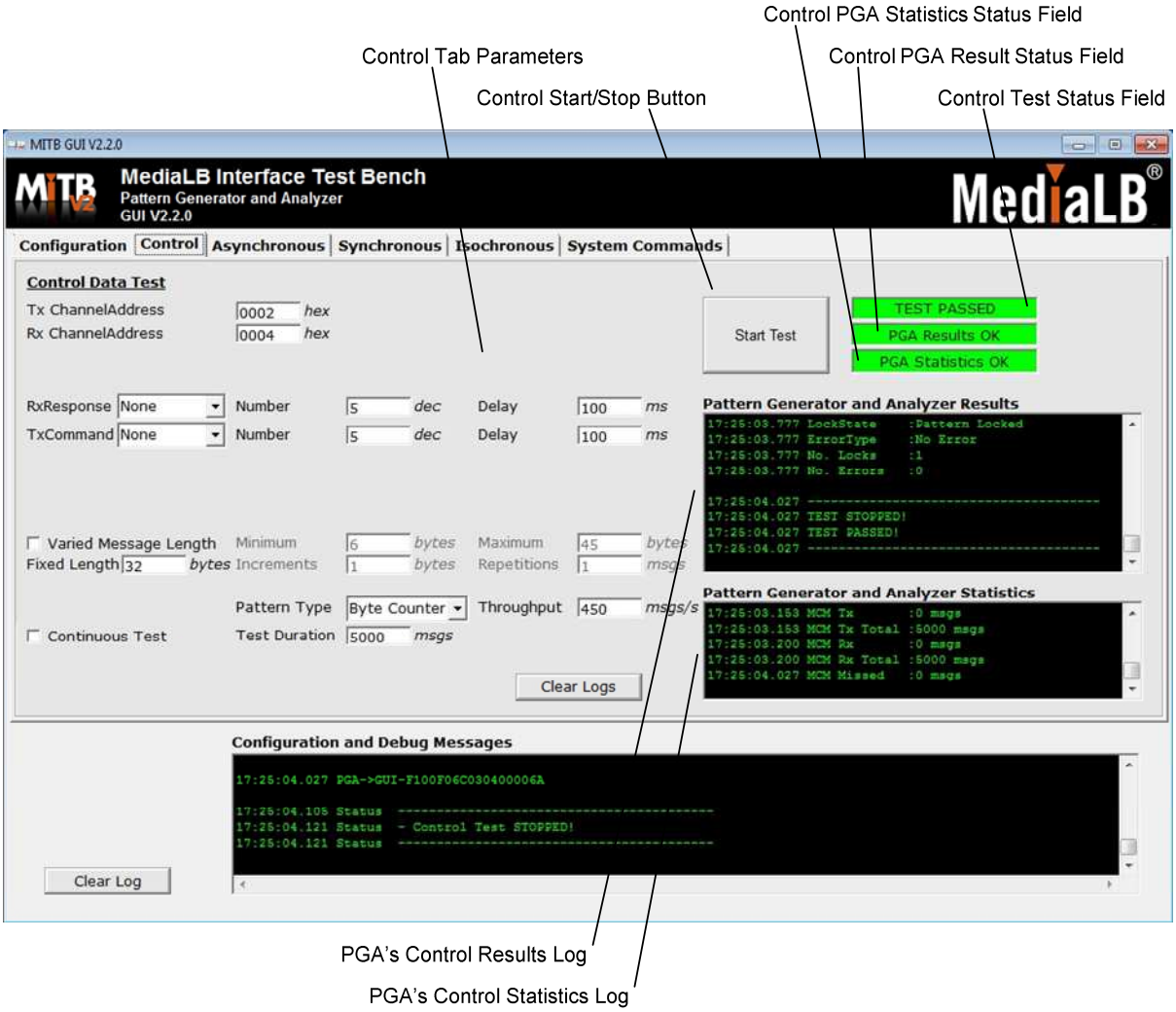

Figure 6-3: Control Tab

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6.2.2.1 Control Tab Parameters

Parameters and buttons of the control tab are described in the table below.

Name	Description
Tx ChannelAddress	MediaLB ChannelAddress on which the control test pattern is transmitted by the OS81110 connected to the MDUT.
Rx ChannelAddress	MediaLB ChannelAddress on which the control test pattern is received by the OS81110 connected to the MDUT.
RxResponse	Defines special RxResponse to be generated by the MITB. The following RxResponses are defined: *None, RxBusy, RxBreak, and RxProtErr*.
RxResponse Number	Indicates number of special RxResponses to be generated.
RxResponse Delay	Indicates approximate delay between consecutive generated RxResponses in ms.
TxCommand	Defines special TxCommands to be generated by the MITB. The following TxCommands are defined: *None, CtrlBreak*.
TxCommand Number	Indicates number of special TxCommands to be generated.
TxComand Delay	Indicates approximate delay between consecutive generated TxCommands in ms.
Varied Message Length	Check box to enable/disable messages with fixed or varied length.
Fixed Length	Length of control messages in case Varied Packet Length is disabled. Value Range: 6- 45 Bytes.
Minimum	Minimum length of control messages in case Varied Packet Length is enabled. Value Range: 6- 45 Bytes, with Minimum < Maximum
Maximum	Maximum length of control messages in case Varied Packet Length is enabled. Value Range: 6- 45 Bytes, with Maximum > Minimum
Increments	Number of bytes the length of consecutive messages are incremented in case Varied Packet Length is enabled.
Repetitions	Number of consecutive messages generated with the same length in case Varied Packet Length is enabled.
Pattern Type	Two types of patterns are supported: *Byte Counter* and *Random*. For details about pattern formats refer to chapter 7.
Throughput	Number of messages transmitted per second. Value Range: 15- 450 msgs/s
Continuous Test	Check box to enable/disable the successive transmission of control messages.
Test Duration	If Continuous Test is disabled the Test Duration defines how many messages are transmitted.
Clear Logs	Button to clear the PGA Results and Statistics windows
Start /Stop Test	Button to manually start and stop the test
Test Status Field	The Control Test Status Field provides an indication of the overall state of a test. The state is indicated by four colors: - Grey: "No Test!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "TEST FAILED" - Test is stopped and failed with errors detected in either the PGA Results or Statistics. - Green: "TEST PASSED" - Test is stopped and passed.
PGA Results Status Field	The Control Results Status Field provides an indication of the PGA test results of actually received test patterns. The state is indicated by four

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	colors: - Grey: "No PGA Results!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "PGA Results NOT OK!" - Test is stopped. Test failed with Pattern Errors (as indicated in the PGA Results window). - Green: "PGA Results OK!" - Test is stopped. No pattern errors in received messages detected.
PGA Statistics Status Field	The Control Statistics Status Field provides an indication of the PGA test statistics. The state is indicated by four colors: - Grey: "No PGA Statistics!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "PGA Statistics NOT OK!" - Test is stopped. Test failed with uneven number of transmitted and received messages. - Green: "PGA Statistics OK!" - Test is stopped. Number of transmitted and received messages equal.

Table 6-3: Control Tab Parameters

6.2.2.2 Control Results Log

The PGA's Control Results Log displays information about the pattern analyzer's state and provides error indications. The information displayed in the Control Results Log is described in the following table.

Name	Description
DataType	ControlMsg_MCM: PGA configured for transfer of MCM
Port	MediaLB: Port used to transfer messages
ReportType	Once: Result report is generated once. Forever: Result report is generated successive.
TimeWindow	1 s: If test is started manually, the period used to generate the result report is 1 s. x s: If test is started by loading a configuration file, the period used to generate the result report is defined in the loaded file.
LockState	Pattern Unlock: Pattern Analyzer receives invalid messages. Pattern Search: Pattern Analyzer received a valid message and waits to receive the next message in the correct sequence. Pattern Locked: Pattern Analyzer receives valid messages.
ErrorType	No Error: No error detected. Corrupted Msg: Message incorporates error in payload. Missed Msg: Error in received message sequence detected.
No. Locks	Number of transitions from unlock to lock state
No. Errors	Number of detected errors
Cnt Index	Message counter value on which an error was detected.
Index	Byte number pointing to start of quadlet on which an error was detected.
Read Value	Received message counter value
Exp Value	Expected message counter value

Table 6-4: Control Results Log

A successful control data test indicates:

- No. Locks : 1
- No. Errors : 0
- MCM Missed : 0 msgs

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The test result is indicated on the test status field next to the Start/Stop Button as soon as a test is stopped.

6.2.2.3 Control Statistics Log

The PGA's Control Statistics Log displays information about transmitted, received and missed packets. The values displayed in the Control Statistic Log are described in the following table.

Name	Description
MCM Tx	Number of messages transmitted in TimeWindow
MCM Tx Total	Total number of messages transmitted from beginning of test
MCM Rx	Number of messages received in TimeWindow
MCM Rx Total	Total number of messages received from beginning of test
MCM Missed	Total number of missed messages (~ MCM Tx Total – MCM Rx Total)

Table 6-5: Control Statistics Log

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6.2.3 Asynchronous Tab

The following figure shows the asynchronous tab of the GUI. In this tab parameters can be entered, which define the characteristics of the generated asynchronous test patterns. A button is available to manually start and stop the pattern processing. Log windows display the PGA results and statistics. Dedicated test status fields indicate the test status.

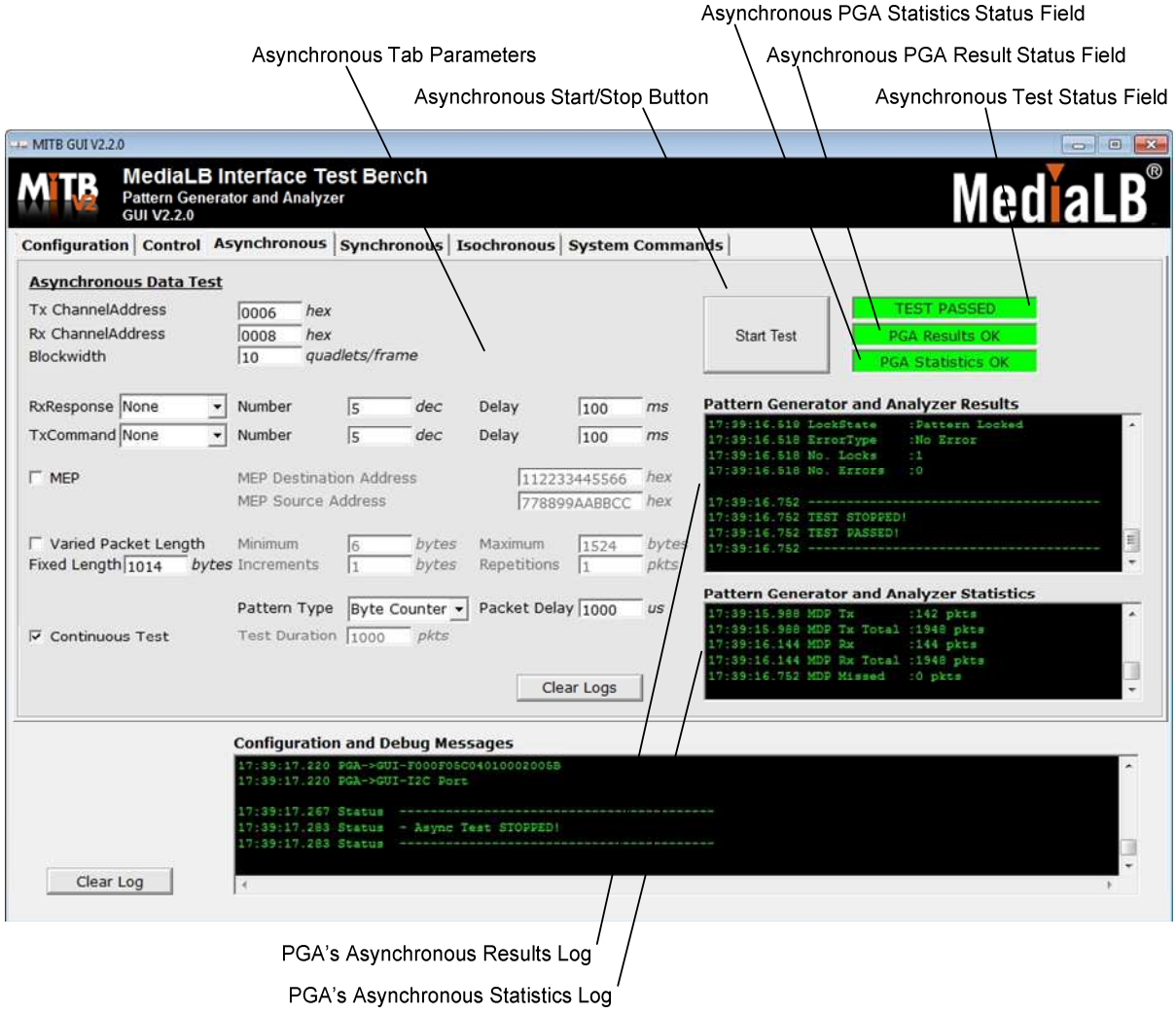

Figure 6-4: Asynchronous Tab

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6.2.3.1 Asynchronous Tab Parameters

Parameters and buttons of the asynchronous tab are described in the table below.

Name	Description
Tx ChannelAddress	MediaLB ChannelAddress on which the asynchronous test pattern is transmitted by the OS81110 connected to the MDUT.
Rx ChannelAddress	MediaLB ChannelAddress on which the asynchronous test pattern is received by the OS81110 connected to the MDUT.
Blockwidth	Number of quadlets allocated per MediaLB frame for the transmission and reception of the asynchronous test pattern. Depending on the MediaLB speed the bandwidth ranges from 1 to 27 quadlets per frame.
RxResponse	Defines special RxResponse to be generated by the MITB. The following RxResponses are defined: *None, RxBusy, RxBreak, and RxProtErr*.
RxResponse Number	Indicates number of special RxResponses to be generated.
RxResponse Delay	Indicates approximate delay between consecutive generated RxResponses in ms.
TxCommand	Defines special TxCommands to be generated by the MITB. The following TxCommands are defined: *None, AsyncBreak*.
TxCommand Number	Indicates number of special TxCommands to be generated.
TxComand Delay	Indicates approximate delay between consecutive generated TxCommands in ms.
MEP	Check box to enable/disable the transfer of MOST Ethernet packets.
MEP Destination Address	48-bit destination address of MOST Ethernet packet
MEP Source Address	48-bit source address of MOST Ethernet packet
Varied Packet Length	Check box to enable/disable packets with fixed or varied length.
Fixed Length	Length of asynchronous packets in case Varied Packet Length has been disabled. Value Range: 6- 1524 Bytes.
Minimum	Minimum length of asynchronous packets in case Varied Packet Length has been enabled. Value Range: 6- 1524 Bytes with Minimum < Maximum
Maximum	Maximum length of asynchronous packets in case Varied Packet Length has been enabled. Value Range: 6- 1524 Bytes with Maximum > Minimum
Increments	Number of bytes the length of consecutive packets are incremented in case Varied Packet Length has been enabled.
Repetitions	Number of consecutive packets generated with the same length in case Varied Packet Length has been enabled.
Pattern Type	Two types of patterns are supported: *Byte Counter* and *Random*. For details about pattern formats refer to chapter 7.
Packet Delay	Defines the delay between the end of a transmitted packet and the start of the following packet. This value is only valid in case the configured Packet delay is higher than the transfer time of the generated packets. Minimum packet delay 1000 us, maximum up to 65535 us.
Continuous Test	Check box to enable/disable the successive transmission of asynchronous packets.
Test Duration	If Continuous Test has been disabled, the Test Duration defines how many packets are transmitted.
Clear Logs	Button to clear the PGA Results and Statistics windows
Start/Stop Test	Button to manually start and stop the test
Test Status Field	The Async Test Status Field provides an indication of the overall state of a test. The state is indicated by four colors:

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	- Grey: "No Test!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "TEST FAILED" - Test is stopped and failed with errors detected in either the PGA Results or Statistics. - Green: "TEST PASSED" - Test is stopped and passed.
PGA Results Status Field	The Async Results Status Field provides an indication of the PGA test results of actually received test patterns. The state is indicated by four colors: - Grey: "No PGA Results!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "PGA Results NOT OK!" - Test is stopped. Test failed with Pattern Errors (as indicated in the PGA Results window). - Green: "PGA Results OK!" - Test is stopped. No pattern errors in received packets detected.
PGA Statistics Status Field	The Async Statistics Status Field provides an indication of the PGA test statistics. The state is indicated by four colors: - Grey: "No PGA Statistics!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "PGA Statistics NOT OK!" - Test is stopped. Test failed with uneven number of transmitted and received packets. - Green: "PGA Statistics OK!" - Test is stopped. Number of transmitted and received packets equal.

Table 6-6: Asynchronous Tab Parameters

6.2.3.2 Asynchronous Results Log

The PGA's Asynchronous Results Log displays information about the pattern analyzer's state and provides error indications. The information displayed in the Asynchronous Results Log is described in the following table.

Name	Description
DataType	PacketMsg_MDP: PGA configured to transfer MDP PacketMsg_MEP: PGA configured to transfer MEP
Port	MediaLB: Port used to transfer packets
ReportType	Once: Result report is generated once. Forever: Result report is generated successive.
TimeWindow	1 s: If test is started manually, the period used to generate the result report is 1 s. x s: If test is started by loading a configuration file, the period used to generate the result report is defined in the loaded file.
LockState	Pattern Unlock: Pattern Analyzer receives invalid packets. Pattern Search: Pattern Analyzer received a valid packet and waits to receive the next packet in the correct sequence. Pattern Locked: Pattern Analyzer receives valid packets.
ErrorType	No Error: No error detected. Corrupted Msg: Packet incorporates error in payload. Missed Msg: Error in received packet sequence detected.
No. Locks	Number of transitions from unlock to lock state
No. Errors	Number of detected errors.
Cnt Index	Packet-counter value on which an error was detected.
Index	Byte number pointing to start of quadlet on which an error was detected.
Read Value	Received packet counter value
Exp Value	Expected packet counter value

Table 6-7: Asynchronous Results Log

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A successful asynchronous data test indicates:

- No. Locks : 1
- No. Errors : 0
- MDP/MEP Missed : 0 pkts

The test result is indicated on the test status field next to the Start/Stop Button as soon as a test is stopped.

6.2.3.3 Asynchronous Statistics Log

The PGA's Asynchronous Statistics Log displays information about transmitted, received and missed packets. The values displayed in the statistic log are described in the following table.

Name	Description
MDP/MEP Tx	Number of packets transmitted in TimeWindow
MDP/MEP Tx Total	Total number of packets transmitted from start of test
MDP/MEP Rx	Number of packets received in TimeWindow
MDP/MEP Rx Total	Total number of packets received from start of test
MDP/MEP Missed	Total number of missed packets (~ MDP/MEP Tx Total – MDP/MEP Rx Total)

Table 6-8: Asynchronous Statistics Log

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6.2.4 Synchronous Tab

The following figure shows the synchronous tab of the GUI. In this tab parameters can be entered, which define the characteristics of the generated synchronous test patterns. A button is available to manually start and stop the pattern processing. Log windows display the PGA results and statistics. Dedicated test status fields indicate the test status.

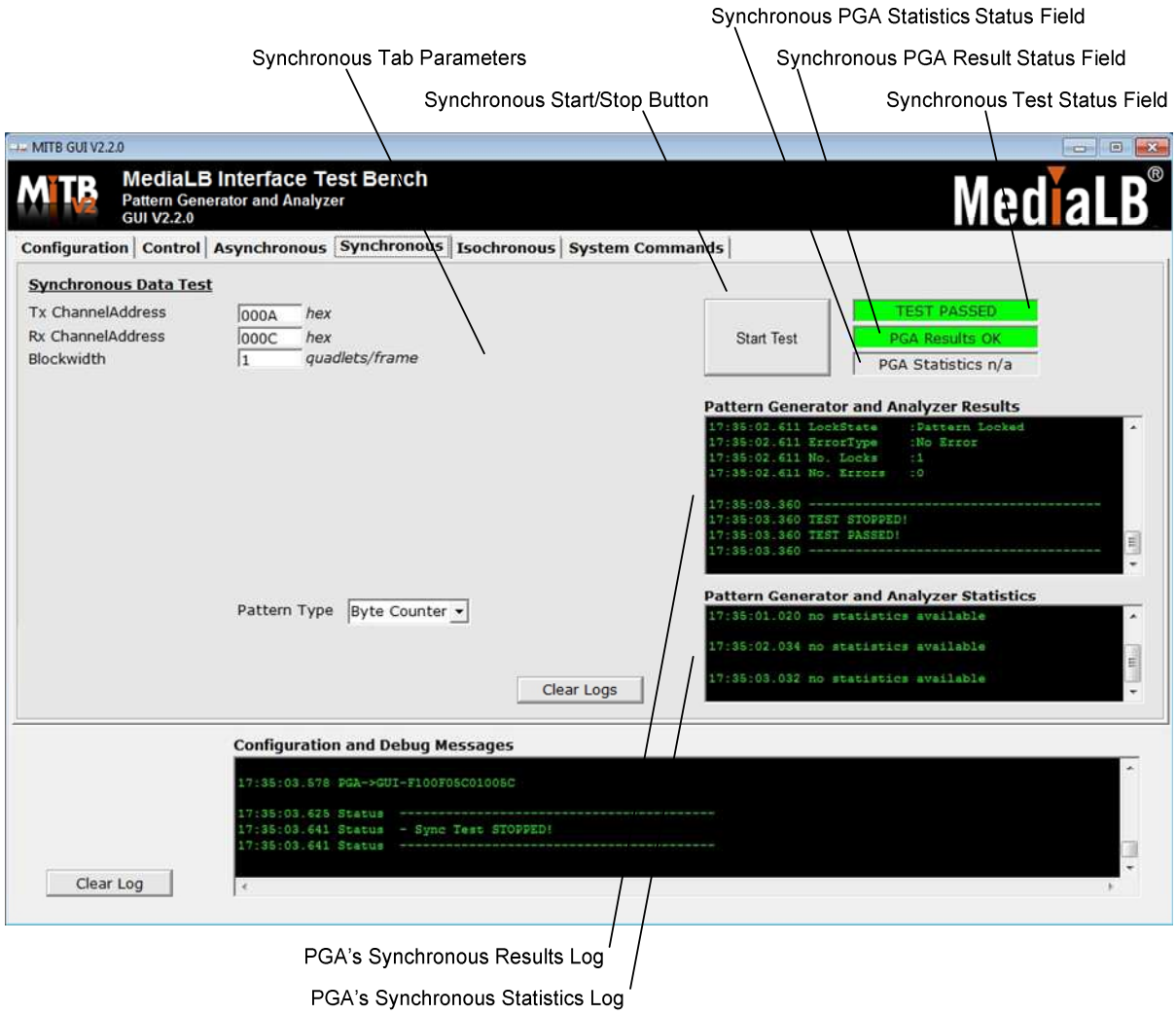

Figure 6-5: Synchronous Tab

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6.2.4.1 Synchronous Tab Parameters

Parameters and buttons of the synchronous tab are described in the table below.

Name	Description
Tx ChannelAddress	MediaLB ChannelAddress on which the synchronous test pattern is transmitted by the OS81110 connected to the MDUT.
Rx ChannelAddress	MediaLB ChannelAddress on which the synchronous test pattern is received by the OS81110 connected to the MDUT.
Blockwidth	Number of quadlets allocated per MediaLB frame for the transmission and reception of the synchronous test pattern. Depending on the MediaLB speed the bandwidth ranges from 1 to 15 quadlets per frame.
Pattern Type	Two types of patterns are supported: *Byte Counter* and *Random*. For details about pattern formats refer to chapter 7.
Clear Logs	Button to clear the PGA Results and Statistics windows
Start/Stop Test	Button to manually start and stop the test
Test Status Field	The Sync Test Status Field provides an indication of the overall state of a test. The state is indicated by four colors: - Grey: "No Test!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "TEST FAILED" - Test is stopped and failed with errors detected in either the PGA Results. - Green: "TEST PASSED" - Test is stopped and passed.
PGA Results Status Field	The Sync Results Status Field provides an indication of the PGA test results of actually received test patterns. The state is indicated by four colors: - Grey: "No PGA Results!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "PGA Results NOT OK!" - Test is stopped. Test failed with Pattern Errors (as indicated in the PGA Results window). - Green: "PGA Results OK!" - Test is stopped. No pattern errors in received stream detected.
PGA Statistics Status Field	The Sync Statistics Status Field is not enabled, since currently there are no PGA statistics available for Synchronous data transfer. - Grey: "PGA Statistics n/a!" - Default state, no PGA statistics available.

Table 6-9: Synchronous Tab Parameters

6.2.4.2 Synchronous Results Log

The PGA's Synchronous Results Log displays information about the pattern analyzer's state and provides error indications. The information displayed in the Synchronous Results Log is described in the following table.

Name	Description
DataType	Sync: PGA configured to transfer synchronous streaming data
Port	MediaLB: Port used to transfer synchronous streaming data
ReportType	Once: Result report is generated once. Forever: Result report is generated successive.
TimeWindow	1 s: If test is started manually, the period used to generate the result report is 1s. x s: If test is started by loading a configuration file, the period used to generate the result report is defined in the loaded file.
LockState	Pattern Unlock: Pattern Analyzer receives invalid synchronous streaming data. Pattern Search: Pattern Analyzer received valid synchronous streaming data and

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	waits to receive the next synchronous data in the correct sequence. Pattern Locked: Pattern Analyzer receives valid synchronous streaming data.
ErrorType	No Error: No error detected. Corrupted Msg: Synchronous streaming data incorporates errors. Missed Msg: Error in received synchronous streaming data sequence detected.
No. Locks	Number of transitions from unlock to lock state
No. Errors	Number of detected errors.
Cnt Index	Frame counter value on which an error was detected.
Index	Byte number pointing to start of quadlet on which an error was detected.
Read Value	Received frame counter value
Exp Value	Expected frame counter value

Table 6-10: Synchronous Results Log

A successful synchronous data test indicates:

- No. Locks : 1
- No. Errors : 0

The test result is indicated on the test status field next to the Start/Stop Button as soon as a test is stopped.

6.2.4.3 Synchronous Statistics Log

For synchronous data no statistics are available.

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6.2.5 Isochronous Tab

The following figure shows the isochronous tab of the GUI. In this tab parameters can be entered, which define the characteristics of the generated isochronous test patterns. A button is available to manually start and stop the pattern processing. Log windows display the PGA results and statistics. Dedicated test status fields indicate the test status.

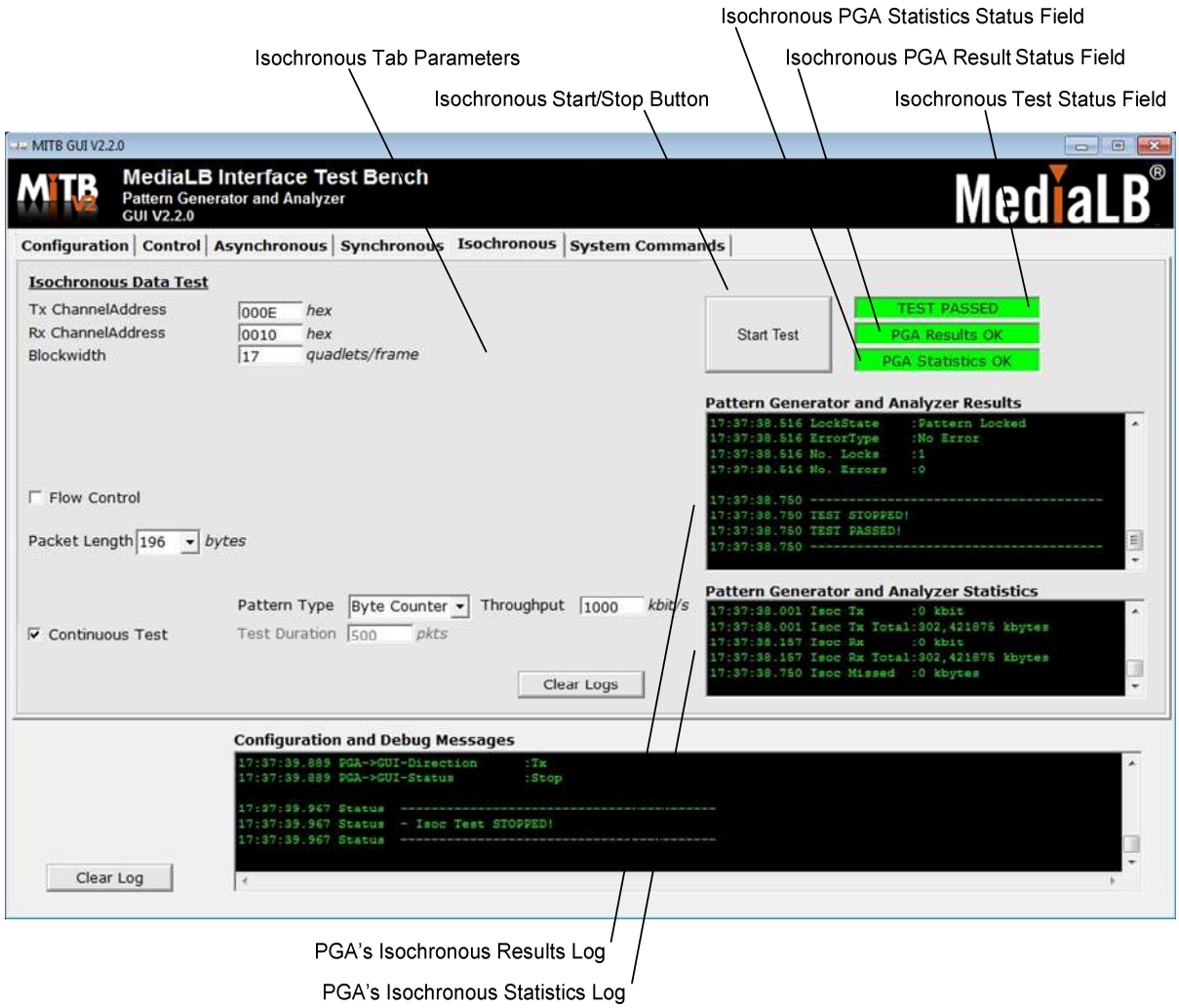

Figure 6-6: Isochronous Tab

6.2.5.1 Isochronous Tab Parameters

Parameters and buttons of the isochronous tab are described in the table below.

Name	Description
Tx ChannelAddress	MediaLB ChannelAddress on which the isochronous test pattern is transmitted by the OS81110 connected to the MDUT.
Rx ChannelAddress	MediaLB ChannelAddress on which the isochronous test pattern is received by the OS81110 connected to the MDUT.
Blockwidth	Number of quadlets allocated per MediaLB frame for the transmission and reception of the isochronous test pattern. Depending on the MediaLB speed the bandwidth ranges from 1 to 27 quadlets per frame.
Flow Control	Check box to enable/disable the generation of RxResponses on an isochronous receive channel of the OS81110 connected to the MDUT.
Packet Length	188: Length of isochronous packet set to 188 bytes 196: Length of isochronous packet set to 196 bytes
Pattern Type	Two types of patterns are supported: *Byte Counter* and *Random* For details about pattern formats refer to chapter 7.
Throughput	Isochronous data (in kbit) transmitted per second. Minimum throughput 1000 kbit/s, maximum up to 65535 kbit/s.
Continuous Test	Check box to enable/disable the successive transmission of isochronous packets.
Test Duration	If Continuous Test has been disabled the Test Duration defines how many packets are transmitted.
Clear Logs	Button to clear the PGA Results and Statistics windows
Start/Stop Test	Button to manually start and stop the test
Test Status Field	The Isoc Test Status Field provides an indication of the overall state of a test. The state is indicated by four colors: - Grey: "No Test!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "TEST FAILED" - Test is stopped and failed with errors detected in either the PGA Results or Statistics. - Green: "TEST PASSED" - Test is stopped and passed.
PGA Results Status Field	The Isoc Results Status Field provides an indication of the PGA test results of actually received test patterns. The state is indicated by four colors: - Grey: "No PGA Results!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "PGA Results NOT OK!" - Test is stopped. Test failed with Pattern Errors (as indicated in the PGA Results window). - Green: "PGA Results OK!" - Test is stopped. No pattern errors in received packets detected.
PGA Statistics Status Field	The Isoc Statistics Status Field provides an indication of the PGA test statistics. The state is indicated by four colors: - Grey: "No PGA Statistics!" - Default state, no active test. - Yellow: "Test Running" - Test active and running. - Red: "PGA Statistics NOT OK!" - Test is stopped. Test failed with uneven number of transmitted and received packets. - Green: "PGA Statistics OK!" - Test is stopped. Number of transmitted and received packets equal.

Table 6-11: Isochronous Tab Parameters

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6.2.5.2 Isochronous Results Log

The PGA's Isochronous Results Log displays information about the pattern analyzer's state and provides error indications. The information displayed in the Isochronous Results Log is described in the following table.

Name	Description
DataType	IsocPacket: PGA configured to transfer isochronous packets
Port	MediaLB: Port used to transfer isochronous packets
ReportType	Once: Result report is generated once. Forever: Result report is generated successive.
TimeWindow	1 s: If test is started manually, the period used to generate the result report is 1s. x s: If test is started by loading a configuration file, the period used to generate the result report is defined in the loaded file.
LockState	Pattern Unlock: Pattern Analyzer receives invalid packets. Pattern Search: Pattern Analyzer received a valid packet and waits to receive the next packet in the correct sequence. Pattern Locked: Pattern Analyzer receives valid packets.
ErrorType	No Error: No error detected. Corrupted Msg: Packet incorporates error in payload. Missed Msg: Error in received packet sequence detected.
No. Locks	Number of transitions from unlock to lock state
No. Errors	Number of detected errors.
Cnt Index	Packet-counter value on which an error was detected.
Index	Byte number pointing to start of quadlet on which an error was detected
Read Value	Received packet counter value
Exp Value	Expected packet counter value

Table 6-12: Isochronous Results Log

A successful isochronous data test indicates:

- No. Locks : 1
- No. Errors : 0

The test result is indicated on the test status field next to the Start/Stop Button as soon as a test is stopped.

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6.2.5.3 Isochronous Statistics Log

The PGA's Isochronous Statistics Log displays information about transmitted, received and missed packets. The values displayed in the Isochronous Statistic Log are described in the following table.

Name	Description
Isoc Tx	Isochronous throughput (in kbit + no. of packets) transmitted in TimeWindow
Isoc Tx Total	Total isochronous throughput (in k/M/GBytes + no. of packets) transmitted from start of test
Isoc Rx	Isochronous throughput (in kbit + no. of packets) received in TimeWindow
Isoc Rx Total	Total isochronous throughput (in k/M/GBytes + no. of packets) received from start of test
Isoc Missed	Total missed isochronous throughput (in k/M/GBytes + no. of packets) (Isoc Tx Total - Isoc Rx Total)

Table 6-13: Isochronous Statistics Log

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6.2.6 System Commands Tab

The following figure shows the system commands tab of the GUI. This tab provides the functionality required to generate MediaLB System Commands.

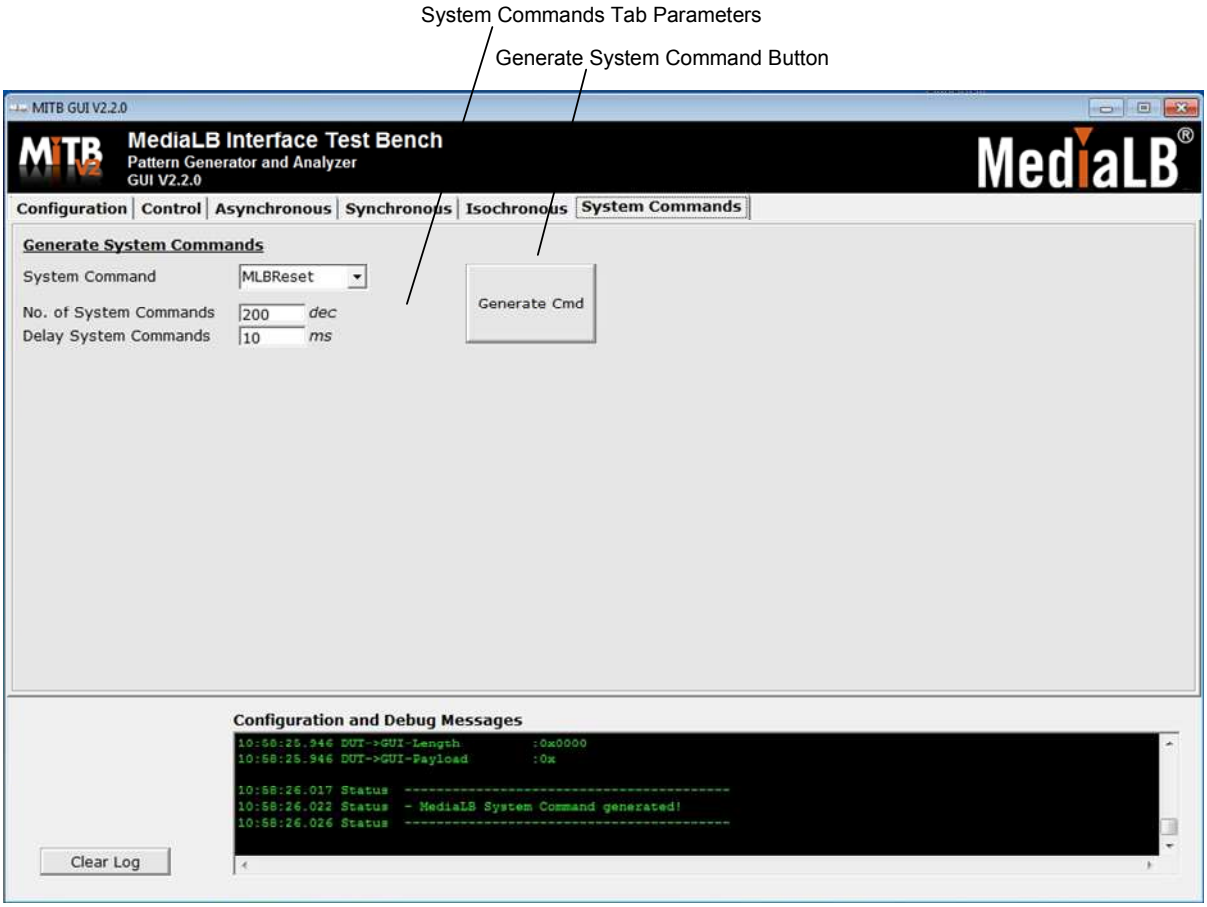

Figure 6-7: System Commands Tab

6.2.6.1 System Commands Tab Parameters

Parameters and buttons of the system commands tab are described in the table below.

Name	Description
System Command	MediaLB System Command to be generated
No. of System Commands	Number of system commands to be generated
Delay System Commands	Approximate delay between the generation of consecutive system commands in ms
Generate Cmd	Button to manually start the generation of the MediaLB System Commands

Table 6-14: System Commands Tab Parameters

Hint Once the “Generate Cmd” button is clicked, the generation of System Commands is stopped after the number of adjusted commands is generated or the “Initialize MITB” button on the configuration tab has been clicked.

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6.3 Configuration Sequence

To configure the MITB and execute a test two approaches are possible:

- **Manual configuration**
- **Load configuration files**

Both approaches are described in detail in the following sections.

6.3.1 Manual Configuration

At manual configuration the user needs to enter the test parameters on the GUI. Tests are started and terminated by clicking the respective Start/Stop button.

For manual configuration the following sequence is recommended:

Step 1: Configure MITB
- **Step 1.1:** Select configuration tab, see Figure 6-2.
- **Step 1.2:** Define RS232 Port.
- **Step 1.3:** Select MDUT MediaLB Interface Mode (3-Pin or 6-Pin).
- **Step 1.4:** Select MDUT MediaLB Clock Speed (256xFs, 512xFs…).
- **Step 1.5:** Select MDUT MOST Target Address (typically 0101hex).
- **Step 1.6:** Enable or disable Trigger on Error events.
- **Step 1.7:** Enable or disable visibility of Configuration/Debug Messages.
- **Step 1.8:** Click “Initialize MITB” button to configure MITB with the provided parameters.

Step 2: Configure Test Pattern
- **Step 2.1:** Select tab for required data type, see Figure 6-6.
- **Step 2.2:** Select and enter data type specific parameters.

Step 3: Start Loop-Back Application on Device Under Test

To successfully run a test make sure that the MDUT is configured for the same parameters as adjusted on the GUI and the loop-back function has been enabled.

Step 4: Execute Test
- **Step 4.1:** Click “Start Test” button to activate pattern generation.
- **Step 4.2:** Wait until number of expected test patterns are generated.
- **Step 4.3:** Click “Stop Test” button to hold pattern generation.

Step 5: Verify Test Results
- **Step 5.1:** Check error log of result log and/or test status field.

Step 6: Re-run Test

If MediaLB specific parameters such as interface mode or clock speed need to be modified, go to Step 1. If modifications of data pattern specific parameters or no modifications at all are required, go to Step 2.

Note Manual configuration does not support concurrent pattern generation of different data types.

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6.3.2 Load Configuration Files

The MITB includes a set of predefined test cases. For every test case a configuration setup file is provided, which is used to initialize the MITB. Additionally, for every test case a configuration file is available to start the generation of test patterns. The provided configuration files include all parameters required to execute a defined test.

The configuration files for the predefined test cases are part of the MITB delivery and can be found on the installation CD. For details about the files provided on the installation CD refer to chapter 9, Summary of Provided Files.

For loading the configuration files the following sequence is recommended:

Step 1: Configure MITB
- **Step 1.1:** Select configuration tab, see Figure 6-2.
- **Step 1.2:** Define RS232 Port.
- **Step 1.3:** Enable or disable Trigger on Error events.
- **Step 1.4:** Enable or disable visibility of Configuration/Debug Messages.
- **Step 1.5:** Click “Initialize MITB” button to configure MITB with the provided parameters.
- **Step 1.6:** Select predefined test case to be executed.
- **Step 1.7:** Click “Load Config File” button and load setup file for selected test case.

Step 2: Start Loop-Back Application on Device Under Test

To successfully run a test make sure that the MDUT is configured for the same parameters as adjusted on the GUI and the loop-back function has been enabled.

Step 3: Execute Test
- **Step 3.1:** Click “Load Config File” button and load start file for selected test case.
- **Step 3.2:** Wait until number of expected test patterns are generated.
- **Step 3.3:** Click “Stop Test” button to hold pattern generation.

Step 4: Verify Test Results
- **Step 4.1:** Check error log of result log and/or test status field.

Step 5: Re-run Test

To re-run the test, click the “Start Test” button and go to Step 3.2.

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6.4 Log Files

The GUI generates several log files. The files store the content of the log windows and are saved in the folder which contains the *MITB_GUI_V02_02_XX.exe* file.

If no test configuration file is loaded on the GUI the following log files are created:

- *log_cfg.txt*: Includes configuration and debug messages
- *log_pga_ctrl.txt:* Includes PGA results and statistics of control data test
- *log_pga_async.txt:* Includes PGA results and statistics of asynchronous data test
- *log_pga_sync.txt:* Includes PGA results and statistics of synchronous data test
- *log_pga_isoc.txt:* Includes PGA results and statistics of isochronous data test

If a configuration file for a specific test case is loaded on the GUI, log files, incorporating the test name as prefix, are created:

- *log_cfg.txt* Includes configuration and debug messages of MITB initialization
- *mitb_t…_log_cfg.txt*: Includes configuration and debug messages
- *mitb_t…_log_pga_ctrl.txt:* Includes PGA results and statistics of control data test
- *mitb_t…_log_pga_async.txt*: Includes PGA results and statistics of asynchronous data test
- *mitb_t…_log_pga_sync.txt* Includes PGA results and statistics of synchronous data test
- *mitb_t…_log_pga_isoc.txt* Includes PGA results and statistics of isochronous data test

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7 Test Pattern Formats

The MITB transfers MediaLB test pattern, which are received and re-transmitted by the MDUT.

Test patterns of the following data type are supported by the MITB:

- Control messages
- Asynchronous packets
- Synchronous streaming data
- Isochronous packets

The format of the pattern for the various supported data types are described in the following sections.

7.1 Control Message Format

Control data is transferred in messages. The MITB supports the generation of control messages with a maximum length of 58 bytes. The control message format is defined below:

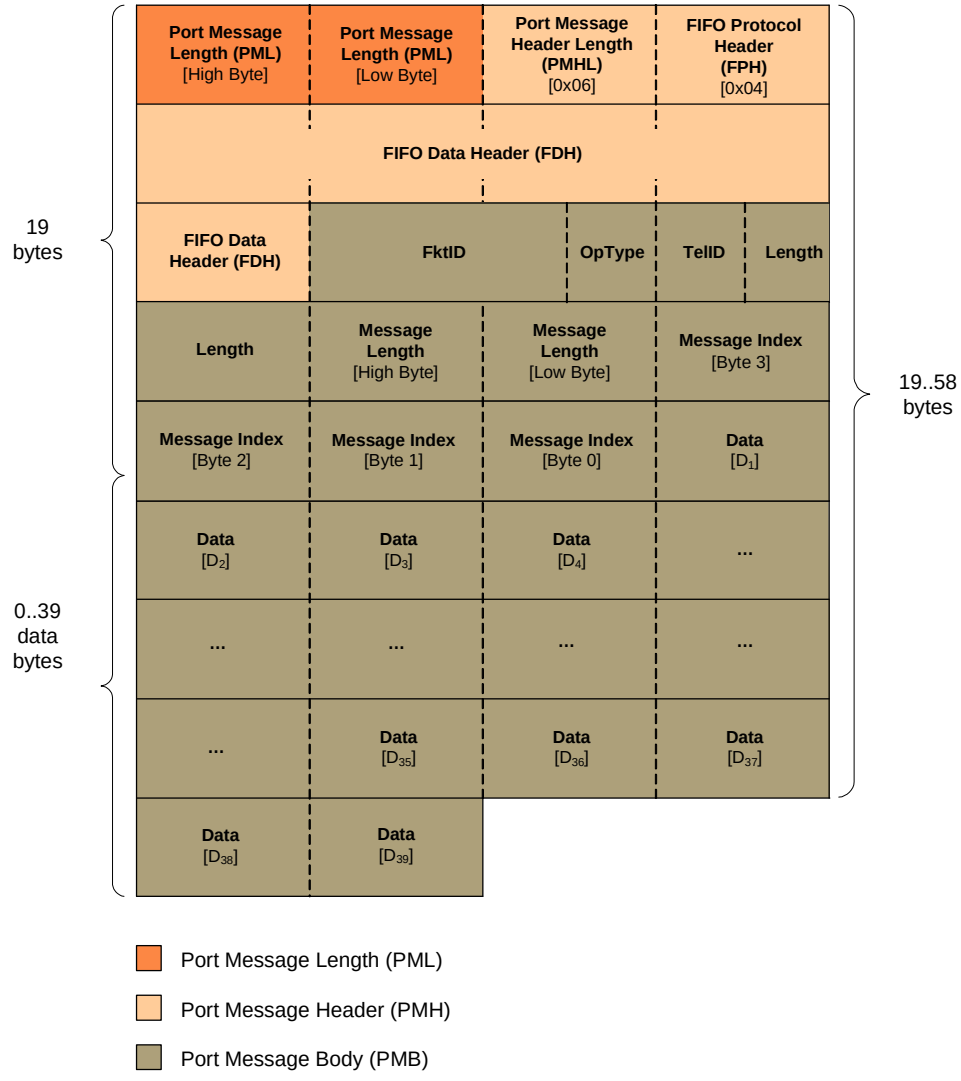

Figure 7-1: Control Message Format

Name	Description
PML	16-bit field indicating the total number of bytes that follow in the Port Message Header (PMH) and the Port Message Body (PMB)
PMHL	Single byte field indicating the byte length of the FIFO Protocol Header (FPH) and FIFO Data Header (FDH). Value is always set to 0x06.
FPH	Defines the Port Message Type and the FIFO to be targeted. Value is always set to 0x04.
FDH	For definition of the FIFO Data Header refer to the INIC User's Manual [6].
FktID	12-bit segment. Value is always set to 0xF00.
OpType	4-bit segment. Value is always set to 0x0.
TelID	4-bit segment. Value is always set to 0x0.
Length	12-bit field indicating the total number of data bytes following in the Port Message Body (PMB)
Message Length	16-bit field indicating the total number of bytes which follow in the Port Message Body (PMB) including the two bytes of Message Length itself. Message Length can be adjusted in the MITB GUI. Minimum value: **6** bytes Maximum value: **45** bytes
Message Index	32-bit field representing a message counter which is incremented for each transmitted message.

Data	Data bytes with pattern type: Byte Counter or Random.
	Number of data bytes can vary from 0 to 39 bytes.
	
	Pattern Type: **Byte Counter**
	`| Message Index | Data`
	`Message 1: ... | 00 00 00 00 | 04 05 06 07 08 09 ...`
	`Message 2: ... | 00 00 00 01 | 05 06 07 08 09 0A ...`
	`Message 3: ... | 00 00 00 02 | 06 07 08 09 0A 0B ...`
	`...`
	
	Pattern Type: **Random**
	`| Message Index | Data`
	`Message 1: ... | 00 00 00 00 | F8 66 99 4F E0 AB ...`
	`Message 2: ... | 00 00 00 01 | 60 33 BC 0E 56 69 ...`
	`Message 3: ... | 00 00 00 02 | 8C 26 89 7E 8D 77 ...`
	`...`

Table 7-1: Control Message Format Description

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7.2 Asynchronous Packet Format

Asynchronous data is transferred in packets. The MITB supports the generation of MOST Data Packets (MDPs) and MOST Ethernet Packets (MEPs).

The format of MDPs and MEPs is described in the following sections.

7.2.1 MOST Data Packets (MDPs)

MDPs support a maximum packet length of 1534 bytes. The MDP format is depicted below:

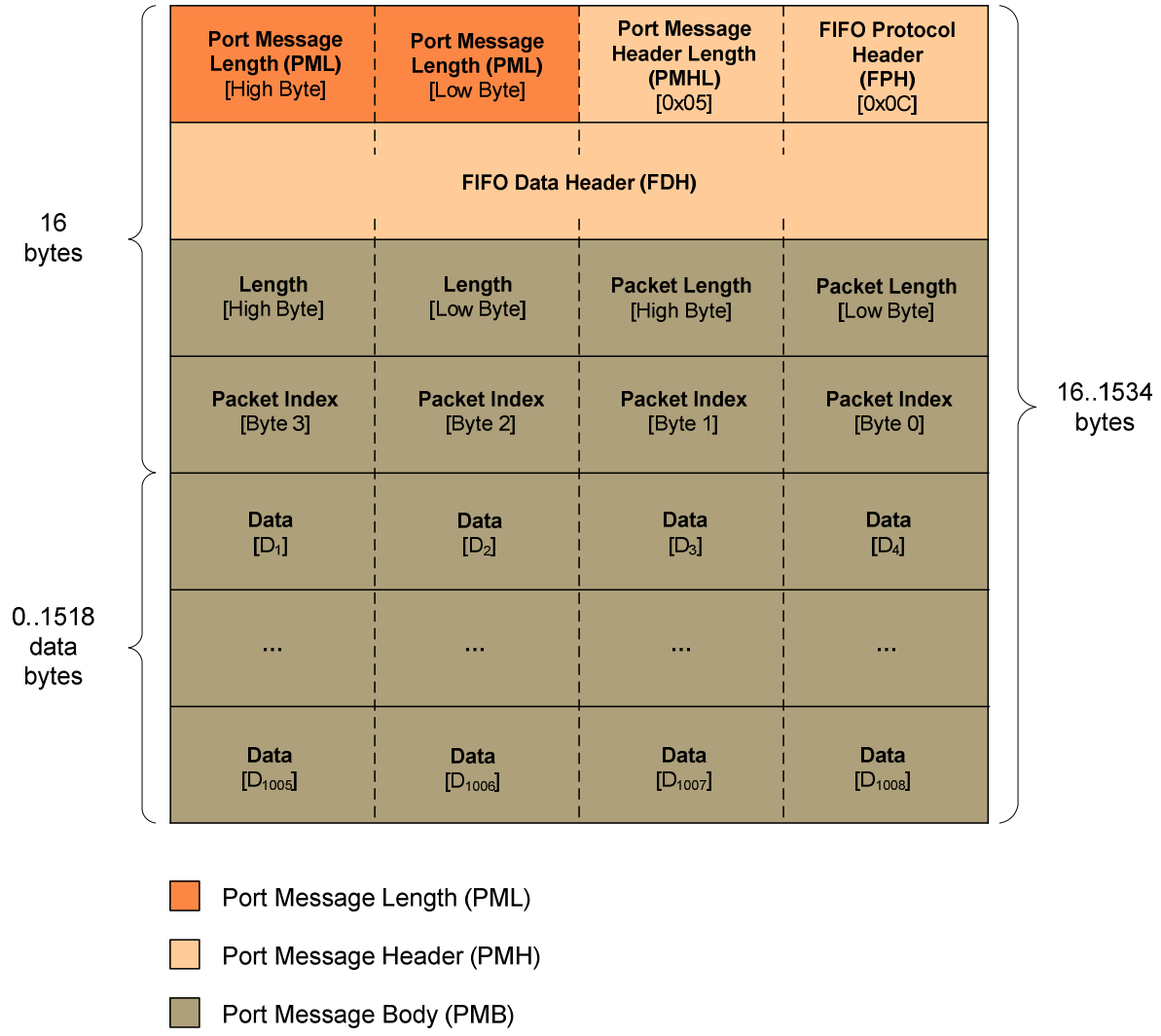

Figure 7-2: Data Packet Format

Name	Description
PML	16-bit field indicating the total number of bytes that follow in the Port Message Header (PMH) and the Port Message Body (PMB)
PMHL	Single byte field indicating the byte length of the FIFO Protocol Header (FPH) and FIFO Data Header (FDH). Value is always set to 0x05.
FPH	Defines the Port Message Type and the FIFO to be targeted. Value is always set to 0x0C.
FDH	For definition of the FIFO Data Header refer to the INIC User's Manual [6].
Length	16-bit field indicating the total number of data bytes following in the Port Message Body (PMB)
Packet Length	16-bit field indicating the total number of bytes which follow in the Port Message Body (PMB) including the two bytes of Packet Length itself. Packet Length can be adjusted in the MITB GUI. Minimum value: **6** bytes Maximum value: **1534** bytes ***Note*** Typically Length and Packet Length are identical. Only in error case it may happen, that length fields don't match!
Packet Index	32-bit field representing a packet counter which is incremented for each transmitted packet.
Data	**Data**: Data bytes with pattern type: Byte Counter or Random. Number of data bytes can vary from 0 to 1518 bytes. Pattern Type: **Byte Counter** `| Packet Index	Data` `Packet 1: ...	00 00 00 00	04 05 06 07 08 09 ...` `Packet 2: ...	00 00 00 01	05 06 07 08 09 0A ...` `Packet 3: ...	00 00 00 02	06 07 08 09 0A 0B ...` `...`  Pattern Type: **Random** `| Packet Index	Data` `Packet 1: ...	00 00 00 00	F8 66 99 4F E0 AB ...` `Packet 2: ...	00 00 00 01	60 33 BC 0E 56 69 ...` `Packet 3: ...	00 00 00 02	8C 26 89 7E 8D 77 ...` `...`

Table 7-2: MDP Format Description

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7.2.2 MOST Ethernet Packets (MEPs)

MEPs support a maximum packet length of 1526 bytes. The MEP format is depicted below:

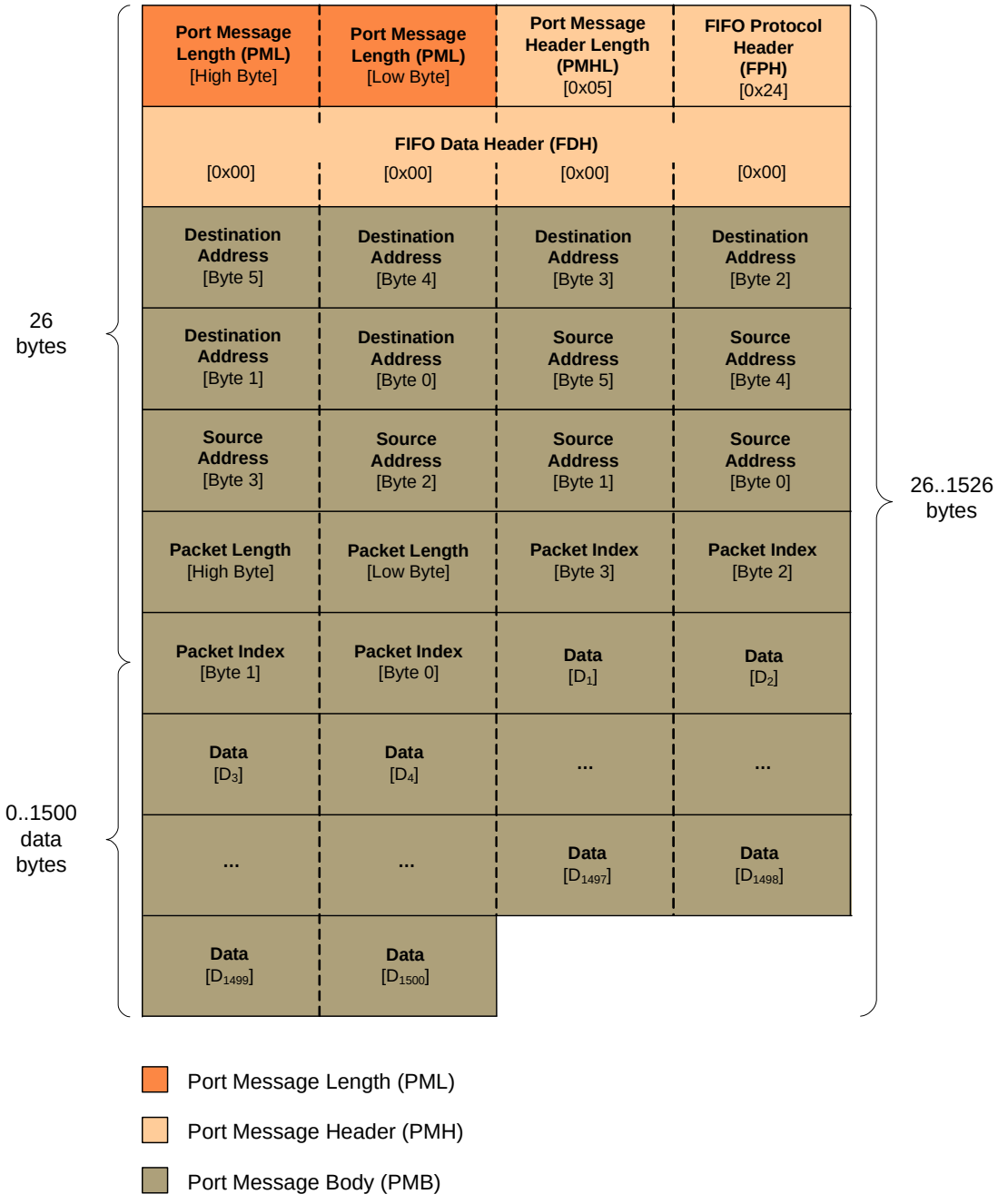

Figure 7-3: Ethernet Packet Format

Name	Description
PML	16-bit field indicating the total number of bytes that follow in the Port Message Header (PMH) and the Port Message Body (PMB)
PMHL	Single byte field indicating the byte length of the FIFO Protocol Header (FPH) and FIFO Data Header (FDH). Value is always set to 0x05.
FPH	Defines the Port Message Type and the FIFO to be targeted. Value is always set to 0x24.
FDH	For MEPs all bytes of the FDH are 0x00.
Destination Address	48-bit field indicating the destination address of the Ethernet device of the MOST network being targeted.
Source Address	48-bit field indicating the source address of the Ethernet device of the MOST network sourcing the packet data.
Packet Length	16-bit field indicating the total number of bytes which follow in the Port Message Body (PMB) including the two bytes of Packet Length itself. Packet Length can be adjusted in the MITB GUI. Minimum value: **6** bytes Maximum value: **1506** bytes
Packet Index	32-bit field representing a packet counter which is incremented for each transmitted packet.

Data	**Data**: Data bytes with pattern type: Byte Counter or Random.
	Number of data bytes can vary from 0 to 1504 bytes.
	
	Pattern Type: **Byte Counter**
	`| Packet Index | Data`
	`Packet 1: ... | 00 00 00 00 | 04 05 06 07 08 09 ...`
	`Packet 2: ... | 00 00 00 01 | 05 06 07 08 09 0A ...`
	`Packet 3: ... | 00 00 00 02 | 06 07 08 09 0A 0B ...`
	`...`
	
	Pattern Type: **Random**
	`| Packet Index | Data`
	`Packet 1: ... | 00 00 00 00 | F8 66 99 4F E0 AB ...`
	`Packet 2: ... | 00 00 00 01 | 60 33 BC 0E 56 69 ...`
	`Packet 3: ... | 00 00 00 02 | 8C 26 89 7E 8D 77 ...`
	`...`

Table 7-3: MEP Format Description

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7.3 Synchronous Pattern Format

Synchronous data is transferred in frames. To identify transferred frames every frame incorporates a 32-bit frame counter in the first quadlet of a frame. The following data bytes support the pattern types: Walking Byte and Random.

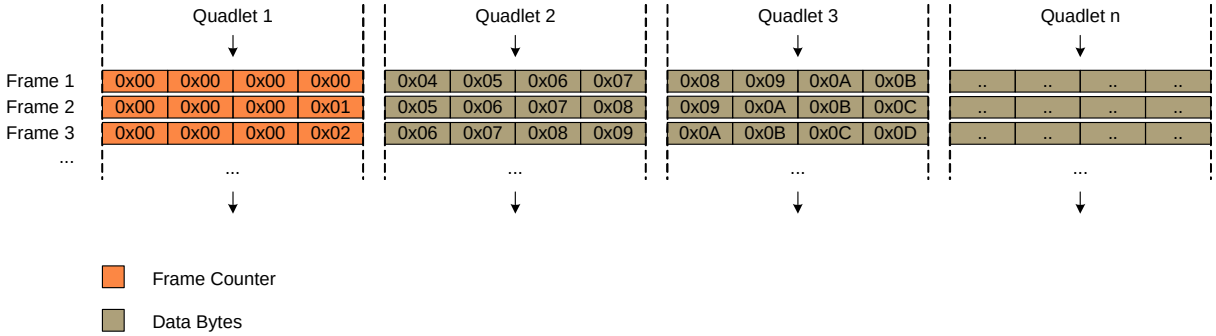

Figure 7-4: Synchronous Byte Counter Format

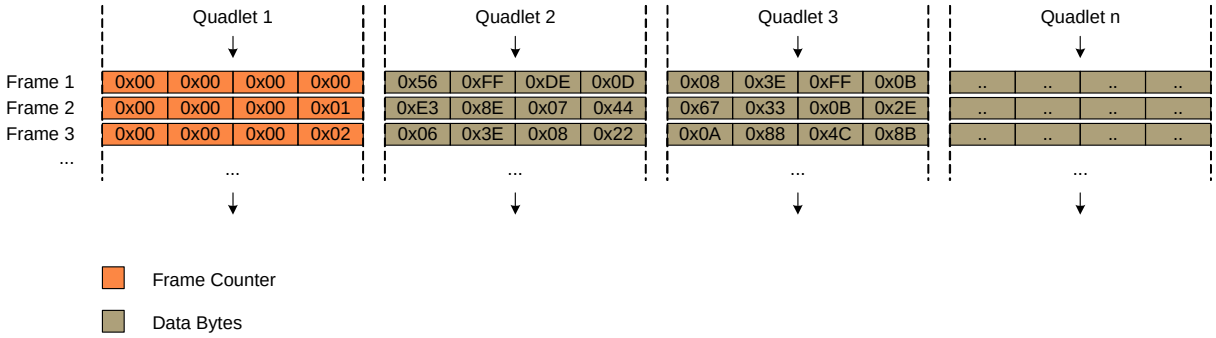

Figure 7-5: Synchronous Random Format

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7.4 Isochronous Packet Format

Isochronous data is transferred in packets. The MITB supports the generation of isochronous packets with the fixed length of 188 bytes or 196 bytes.

To identify transferred packets every packet incorporates a 32-bit packet index. The data bytes support the pattern types: Walking Byte and Random.

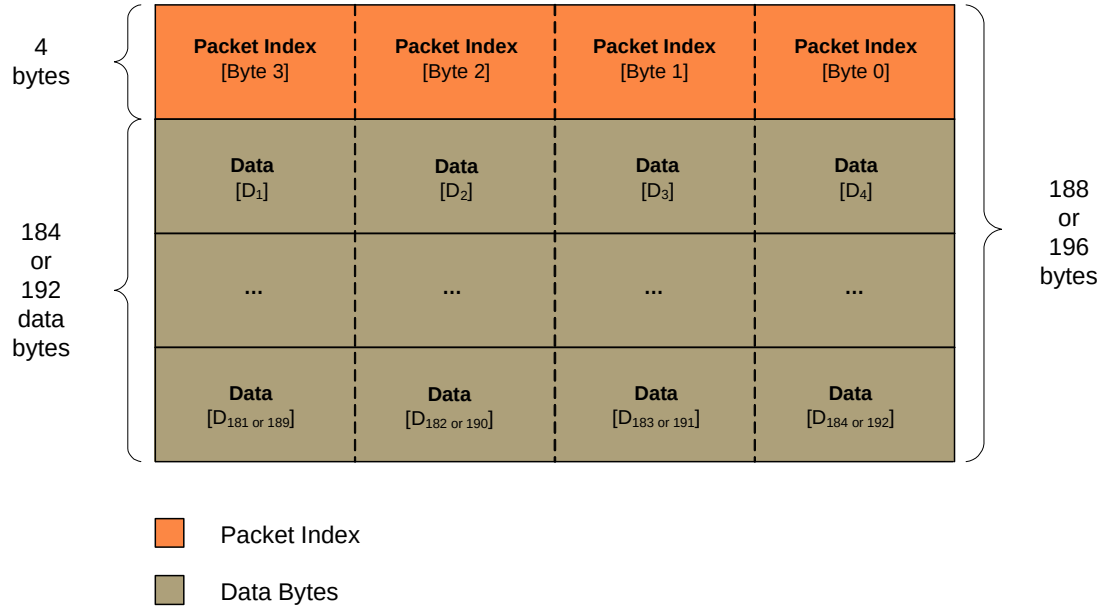

Figure 7-6: Isochronous Packet Format

Name	Description
Packet Index	32-bit field representing a packet counter which is incremented for each transmitted packet

Data	Data bytes with pattern type: Byte Counter or Random.
	Number of data bytes can be adjusted in the GUI to 184 or 192 bytes.
	
	Pattern Type: **Byte Counter**
	`Packet Index | Data`
	`Packet 1: 00 00 00 00 | 04 05 06 07 08 09 ...`
	`Packet 2: 00 00 00 01 | 05 06 07 08 09 0A ...`
	`Packet 3: 00 00 00 02 | 06 07 08 09 0A 0B ...`
	`...`
	
	Pattern Type: **Random**
	`Packet Index | Data`
	`Packet 1: 00 00 00 00 | F8 66 99 4F E0 AB ...`
	`Packet 2: 00 00 00 01 | 60 33 BC 0E 56 69 ...`
	`Packet 3: 00 00 00 02 | 8C 26 89 7E 8D 77 ...`
	`...`

Table 7-4: Isochronous Packet Format Description

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8 Test Definition

The MITB includes a set of defined test cases. The test cases are split in the following categories:

- Control data tests
- Asynchronous data tests
- Synchronous data tests
- Isochronous data test
- Combined tests
- Miscellaneous tests

For every category several test cases are defined. A test case is used to verify the proper transfer of test patterns with a selected data type. Combined test cases support the concurrent transfer of test patterns with multiple data types. In addition to the data type, every test is defined by a set of parameters. Miscellaneous tests cover the generation of system commands.

To run a selected test, the user's Device Under Test needs to be programmed to support a loop-back of the test specific test patterns. For the test specific configuration of the MITB, configuration files are part of a test definition. The configuration files need to be loaded with the MITB GUI as described in section 6.3.2.

The following sections define test cases and test specific parameters.

8.1 Test Name Convention

The naming convention for the defined test cases is as follows:

*mitb_**txxxx**_**I**pin_**SSSS**fs_**T**_**Extension***

txxxx: Unique Test Number

I: MediaLB Interface Mode
3 – 3-Pin Mode
6 – 6-Pin Mode

SSSS: MediaLB Clock Speed
256 – 256xFs
512 – 512xFs
1024 – 1024xFs
2048 – 2048xFs
3072 – 3072xFs
4096 – 4096xFs
6144 – 6144xFs
8192 – 8192xFs

T: Data Transfer Type
c – Control Data
a – Asynchronous Data
s – Synchronous Data
i – Isochronous Data
m – Miscellaneous
Combination of *c, a, s* and *i* in case of combined test cases

Extension: Verbal description (optional)

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8.2 Control Tests

The following table provides an overview of available control data tests.

Overview Control Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t1310_3pin_256fs_c_1q	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 8 Bytes - Throughput 450 msgs/s
mitb_t1320_3pin_512fs_c_1q	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 14 Bytes - Throughput 550 msgs/s
mitb_t1330_3pin_1024fs_c_1q	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 28 Bytes - Throughput 450 msgs/s
mitb_t1331_3pin_1024fs_c_1q	1024xFs test with min. and max. Message Length - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 450 msgs/s
mitb_t1332_3pin_1024fs_c_1q	1024xFs test with maximum Message Throughput - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 475 msgs/s
mitb_t1333_3pin_1024fs_c_1q	1024xFs test with none default ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 475 msgs/s - CA = 0x0012, CA = 0x0026
mitb_t1335_3pin_1024fs_c_1q	1024xFs test with RxBusy Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s

Table 8-1: Control Test Overview (Part 1)

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Overview Control Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t1336_3pin_1024fs_c_1q	1024xFs test with RxBreak Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length45 Bytes - Throughput 500 msgs/s
mitb_t1337_3pin_1024fs_c_1q	1024xFs test with RxProtErr Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s
mitb_t1338_3pin_1024fs_c_1q	1024xFs test with TxBreak Commands generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s
MediaLB 6-pin Tests	
mitb_t1640_6pin_2048fs_c_1q	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 32 Bytes - Throughput 450 msgs/s
mitb_t1641_6pin_2048fs_c_1q	2048xFs test with RxBusy Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s
mitb_t1642_6pin_2048fs_c_1q	2048xFs test with RxBreak Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length45 Bytes - Throughput 500 msgs/s
mitb_t1643_6pin_2048fs_c_1q	2048xFs test with RxProtErr Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s
mitb_t1644_6pin_2048fs_c_1q	2048xFs test with TxBreak Commands generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s

Table 8-2: Control Test Overview (Part 2)

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Overview Control Tests	
Test Name	**Test Characteristics**
MediaLB 6-pin Tests	
mitb_t1650_6pin_3072fs_c_1q	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 14 Bytes - Throughput 250 msgs/s
mitb_t1651_6pin_3072fs_c_1q	3072xFs test with min/max msg length, max throughput - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 475 msgs/s
mitb_t1660_6pin_4096fs_c_1q	Basic 4096xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 14 Bytes - Throughput 250 msgs/s
mitb_t1661_6pin_4096fs_c_1q	4096xFs test with min/max msg length, max throughput - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 475 msgs/s

Table 8-3: Control Test Overview (Part 3)

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8.2.1 mitb_t1310_3pin_256fs_c_1q

Test Name	*mitb_t1310_3pin_256fs_c_1q*						
Description	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 8 Bytes - Throughput 450 msgs/s						
Test Configuration Files	*mitb_t1310_3pin_256fs_c_1q_cfg_setup.txt* *mitb_t1310_3pin_256fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	256xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC7	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	256xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	450	Enable	Byte Counter			

Table 8-4: mitb_t1310_3pin_256fs_c_1q

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8.2.2 mitb_t1320_3pin_512fs_c_1q

Test Name	***mitb_t1320_3pin_512fs_c_1q***						
Description	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 14 Bytes - Throughput 550 msgs/s						
Test Configuration Files	*mitb_t1320_3pin_512fs_c_1q_cfg_setup.txt* *mitb_t1320_3pin_512fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	512xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC15	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	512xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	450	Enable	Byte Counter			

Table 8-5: mitb_t1320_3pin_512fs_c_1q

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8.2.3 mitb_t1330_3pin_1024fs_c_1q

Test Name	*mitb_t1330_3pin_1024fs_c_1q*						
Description	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 28 Bytes - Throughput 450 msgs/s						
Test Configuration Files	*mitb_t1330_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1330_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	28	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	450	Enable	Byte Counter			

Table 8-6: mitb_t1330_3pin_1024fs_c_1q

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8.2.4 mitb_t1331_3pin_1024fs_c_1q

Test Name	*mitb_t1331_3pin_1024fs_c_1q*						
Description	1024xFs test with min. and max. Message Length - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 450 msgs/s						
Test Configuration Files	*mitb_t1331_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1331_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Enable	-	6	45	1	1		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	450	Enable	Byte Counter			

Table 8-7: mitb_t1331_3pin_1024fs_c_1q

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8.2.5 mitb_t1332_3pin_1024fs_c_1q

Test Name	*mitb_t1332_3pin_1024fs_c_1q*						
Description	1024xFs test with maximum Message Throughput - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 500 msgs/s						
Test Configuration Files	*mitb_t1332_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1332_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Enable	-	6	45	1	1		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	475	Enable	Byte Counter			

Table 8-8: mitb_t1332_3pin_1024fs_c_1q

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8.2.6 mitb_t1333_3pin_1024fs_c_1q

Test Name	*mitb_t1333_3pin_1024fs_c_1q*						
Description	1024xFs test with none default ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 500 msgs/s						
Test Configuration Files	*mitb_t1333_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1333_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				…	…		
				PC15	0x0026	Control Tx	
				PC28	0x0012	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0012	0x0026						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Enable	-	6	45	1	1		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	475	Enable	Byte Counter			

Table 8-9: mitb_t1333_3pin_1024fs_c_1q

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8.2.7 mitb_t1335_3pin_1024fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting control data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverBusy* responses.

After the data transfer is started, the MITB will generate a series of 20 consecutive *ReceiverBusy* response periods on the Control Rx Channel (ChannelAddress 0x0002) of the OS81110. During each period, the OS81110 generates *ReceiverBusy* responses in every frame on the Control Rx Channel for approximately 3 ms. After a delay of 500 ms, at which the OS81110 is able to receive data, indicated by *ReceiverReady* responses, the next *ReceiverBusy* period starts.

The *ReceiverBusy* responses indicate that the OS81110 connected to the MDUT is not able to receive data. The *ReceiverBusy* responses need to be detected by the MDUT, and transmitted data quadlets acknowledged by a *ReceiverBusy* response must be repeatedly transmitted until a *ReceiverReady* response is detected. The user must verify this behaviour manually. The MITB does not provide an indication if the *ReceiverBusy* is handled properly by the MDUT.

To verify the MDUT behavior and capture the generated *ReceiverBusy* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverBusy* responses randomly, it cannot be guaranteed, that the *ReceiverBusy* responses always happen at times when the MDUT is transmitting control messages. By that means it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverBusy* responses. It might happen that the *ReceiverBusy* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverBusy* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverBusy* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1335_3pin_1024fs_c_1q indicates a TEST FAILED (with missing messages) in the MITB GUI for most cases. This behavior is expected and is related to the nature of the MOST network and the OS81110.

During the *ReceiverBusy* periods the OS81110 will not receive data from the MDUT via MediaLB. Since loop-back application of the MDUT cannot transmit any data, it also will not be able to receive new messages from the OS81110 via MediaLB and the MITB respectively. This again results in the OS81110 holding of messages received via MOST from the MITB platform. Depending on how long the *ReceiverBusy* period lasts, the OS81110 buffers will run full and messages transmitted from MITB platform to OS81110 via MOST will get lost on the MOST network. There is no such thing as a *ReceiverBusy* response on MOST. Because of this, no feedback from the OS81110 connected to the DUT is passed to the OS81110 on the MITB platform, indicating the buffer full condition of the DUT OS81110 and the MITB keeps transmitting messages, which may get lost.

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Test Name	*mitb_t1335_3pin_1024fs_c_1q*						
Description	1024xFs test with ReceiverBusy responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB generates series of 20 consecutive ReceiverBusy response periods on Control Rx Channel (ChannelAddress 0x0002) of the MDUT OS81110 - During each period ReceiverBusy responses generated in every frame for approximately 3 ms, after delay of 500 ms next ReceiverBusy period starts						
Test Configuration Files	*mitb_t1335_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1335_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Disable	5000	500	Enable	Byte Counter	ReceiverBusy	20	500

Table 8-10: mitb_t1335_3pin_1024fs_c_1q

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8.2.8 mitb_t1336_3pin_1024fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting control data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverBreak* responses.

After the data transfer is started, the MITB will generate 48 *ReceiverBreak* responses on the Control Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverBreak* responses are generated with a delay of 200 ms between consecutive *ReceiverBreak*s.

The MDUT transmitting control messages needs to detect the *ReceiverBreak* responses. Following the detection of the *ReceiverBreak* the MDUT must stop message transmission. The user needs to verify manually, that the MDUT is properly terminating the message transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverBreak* response is signalled. The MITB does not provide an indication if the MDUT is handling the *ReceiverBreak*s as expected.

To verify the MDUT behavior and capture the generated *ReceiverBreak* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverBreak* responses randomly, it cannot be guaranteed, that the *ReceiverBreak* responses always happen at times when the MDUT is transmitting control messages. By that means, it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverBreak* responses. It might happen that the *ReceiverBreak* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverBreak* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverBreak* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1336_3pin_1024fs_c_1q indicates a TEST FAILED (with missing messages) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific DUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverBreak* response, message reception is terminated and the broken message will be lost. In case the MDUT does not re-transmit the broken message, the MITB will indicate a missing message and TEST FAILED. If the broken message is re-transmitted by the MDUT after receiving the *ReceiverBreak* response, the MITB will not detect any errors.

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Test Name	*mitb_t1336_3pin_1024fs_c_1q*						
Description	1024xFs test with ReceiverBreak responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB generates 48 ReceiverBreak responses on the Control Rx Channel (ChannelAddress 0x0002) of the MDUT OS81110 - ReceiverBreak responses generated with a delay of 200 ms between consecutive ReceiverBreaks						
Test Configuration Files	*mitb_t1336_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1336_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Disable	5000	500	Enable	Byte Counter	ReceiverBreak	48	200

Table 8-11: mitb_t1336_3pin_1024fs_c_1q

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8.2.9 mitb_t1337_3pin_1024fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting control data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverProtocolError* responses.

After the data transfer is started, the MITB will generate 20 *ReceiverProtocolError* responses on the Control Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverProtocolError* responses are generated with a delay of 100 ms between consecutive *ReceiverProtocolError*.

The MDUT transmitting control messages needs to detect the *ReceiverProtocolError* responses. Following the detection of the *ReceiverProtocolError* the MDUT must stop message transmission following the MediaLB protocol defined in the MediaLB spec. The user needs to verify manually, that the MDUT is properly terminating the message transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverProtocolError* response is signalled properly. The MITB does not provide an indication if the MDUT is handling the *ReceiverProtocolError* as expected.

To verify the MDUT behavior and capture the generated *ReceiverProtocolError* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverProtocolError* responses randomly, it cannot be guaranteed, that the *ReceiverProtocolError* responses always happen at times when the MDUT is transmitting control messages. By that means, it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverProtocolError* responses. It might happen that the *ReceiverProtocolError* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverProtocolError* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverProtocolError* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1337_3pin_1024fs_c_1q indicates a TEST FAILED (with missing messages) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific MDUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverProtocolError* response, message reception is terminated and the broken message will be lost. In case the MDUT does not re-transmit the broken message, the MITB will indicate a missing message and a TEST FAILED. If the broken message is re-transmitted by the MDUT after receiving the *ReceiverProtocolError* response, the MITB will not detect any errors.

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Test Name	*mitb_t1337_3pin_1024fs_c_1q*						
Description	1024xFs test with ReceiverProtocolErr responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB generates 20 ReceiverProtocolError responses on the Control Rx Channel (ChannelAddress 0x0002) of the DUT OS81110 - ReceiverProtocolError responses generated with a delay of 100 ms between consecutive ReceiverProtocolError						
Test Configuration Files	*mitb_t1337_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1337_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Disable	5000	500	Enable	Byte Counter	ReceiverProtocolError	20	100

Table 8-12: mitb_t1337_3pin_1024fs_c_1q

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8.2.10 mitb_t1338_3pin_1024fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is receiving control data and the transmitting device (OS81110 connected to the MDUT) is sending *ControlBreak* commands.

After the data transfer is started, the MITB will transmit 240 *ControlBreak* command on the Control Tx Channel (ChannelAddress 0x0004) of the OS81110. *ControlBreak* commands are generated with a delay of 20 ms between consecutive *ControlBreak*s.

The MDUT receiving control messages needs to detect the *ControlBreak* commands. Following the detection of the *ControlBreak* the MDUT must stop an ongoing message reception. Already received data quadlets are considered to be invalid and should be rejected. The user needs to verify manually, that the MDUT is properly terminating the message reception. Additionally it may be verified if MDUT internally a status indicating the detection of the *ControlBreak* command is signalled properly. The MITB does not provide an indication if the MDUT is handling the *ControlBreak* as expected.

To verify the MDUT behavior and capture the generated *ControlBreak* command generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ControlBreak* commands randomly, it cannot be guaranteed, that the *ControlBreak* command always happen at times when the OS81110 is transmitting control messages. By that means it is not guaranteed, that the MDUT is receiving a message when the *ControlBreak* command is transmitted by the OS81110. Since the MDUT may not receive a message when the *ControlBreak* is present on the MediaLB bus, the *ControlBreak* command may not be detected by the MDUT. In that case the *ControlBreak* commands have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ControlBreak* command by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1338_3pin_1024fs_c_1q is expected to indicate a TEST PASS. This is the case, because the messages terminated by a *ControlBreak* command are re-transmitted entirely by the OS81110.

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Test Name	*mitb_t1338_3pin_1024fs_c_1q*						
Description	1024xFs test with ControlBreak commands generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB transmits 240 ControlBreak commands on the Control Tx Channel (ChannelAddress 0x0004) of the DUT OS81110 - ControlBreak commands generated with a delay of 20 ms between consecutive ControlBreaks						
Test Configuration Files	*mitb_t1338_3pin_1024fs_c_1q_cfg_setup.txt* *mitb_t1338_3pin_1024fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	TxCmd	Nr. TxCmd	Delay TxCmd (ms)
Disable	5000	500	Enable	Byte Counter	ControlBreak	240	20

Table 8-13: mitb_t1338_3pin_1024fs_c_1q

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8.2.11 mitb_t1640_6pin_2048fs_c_1q

Test Name	*mitb_t1640_6pin_2048fs_c_1q*						
Description	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed 33 Bytes - Throughput 450 msgs/s						
Test Configuration Files	*mitb_t1640_6pin_2048fs_c_1q_cfg_setup.txt* *mitb_t1640_6pin_2048fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…	…	
				…	…	…	
				PC57	0x003E	Unused	
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	32	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	450	Enable	Byte Counter			

Table 8-14: mitb_t1640_6pin_2048fs_c_1q

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8.2.12 mitb_t1641_6pin_2048fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting control data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverBusy* responses.

After the data transfer is started, the MITB will generate a series of 32 consecutive *ReceiverBusy* response periods on the Control Rx Channel (ChannelAddress 0x0002) of the OS81110. During each period, the OS81110 generates *ReceiverBusy* responses in every frame on the Control Rx Channel for approximately 3 ms. After a delay of 500 ms, at which the OS81110 is able to receive data, indicated by *ReceiverReady* responses, the next *ReceiverBusy* period starts.

The *ReceiverBusy* responses indicate that the OS81110 connected to the MDUT is not able to receive data. The *ReceiverBusy* responses need to be detected by the MDUT, and transmitted data quadlets acknowledged by a *ReceiverBusy* response must be repeatedly transmitted until a *ReceiverReady* response is detected. The user must verify this behaviour manually. The MITB does not provide an indication if the *ReceiverBusy* is handled properly by the MDUT.

To verify the MDUT behavior and capture the generated *ReceiverBusy* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverBusy* responses randomly, it cannot be guaranteed, that the *ReceiverBusy* responses always happen at times when the MDUT is transmitting control messages. By that means it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverBusy* responses. It might happen that the *ReceiverBusy* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverBusy* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverBusy* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1641_6pin_2048fs_c_1q indicates a TEST FAILED (with missing messages) in the MITB GUI for most cases. This behavior is expected and is related to the nature of the MOST network and the OS81110.

During the *ReceiverBusy* periods the OS81110 will not receive data from the MDUT via MediaLB. Since loop-back application of the MDUT cannot transmit any data, it also will not be able to receive new messages from the OS81110 via MediaLB and the MITB respectively. This again results in the OS81110 holding of messages received via MOST from the MITB platform. Depending on how long the *ReceiverBusy* period lasts, the OS81110 buffers will run full and messages transmitted from MITB platform to OS81110 via MOST will get lost on the MOST network. There is no such thing as a *ReceiverBusy* response on MOST. Because of this, no feedback from the OS81110 connected to the DUT is passed to the OS81110 on the MITB platform, indicating the buffer full condition of the DUT OS81110 and the MITB keeps transmitting messages, which may get lost.

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Test Name	*mitb_t1641_6pin_2048fs_c_1q*						
Description	2048xFs test with ReceiverBusy responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB generates series of 20 consecutive ReceiverBusy response periods on Control Rx Channel (ChannelAddress 0x0002) of the DUT OS81110 - During each period ReceiverBusy responses generated in every frame for approximately 3 ms, after delay of 500 ms next ReceiverBusy period starts						
Test Configuration Files	*mitb_t1641_6pin_2048fs_c_1q_cfg_setup.txt* *mitb_t1641_6pin_2048fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…	…	
				…	…	…	
				PC57	0x003E	Unused	
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Disable	5000	500	Enable	Byte Counter	ReceiverBusy	20	100

Table 8-15: mitb_t1641_6pin_2048fs_c_1q

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8.2.13 mitb_t1642_6pin_2048fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting control data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverBreak* responses.

After the data transfer is started, the MITB will generate 48 *ReceiverBreak* responses on the Control Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverBreak* responses are generated with a delay of 200 ms between consecutive *ReceiverBreak*s.

The MDUT transmitting control messages needs to detect the *ReceiverBreak* responses. Following the detection of the *ReceiverBreak* the MDUT must stop message transmission. The user needs to verify manually, that the MDUT is properly terminating the message transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverBreak* response is signalled. The MITB does not provide an indication if the MDUT is handling the *ReceiverBreak*s as expected.

To verify the MDUT behavior and capture the generated *ReceiverBreak* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverBreak* responses randomly, it cannot be guaranteed, that the *ReceiverBreak* responses always happen at times when the MDUT is transmitting control messages. By that means, it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverBreak* responses. It might happen that the *ReceiverBreak* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverBreak* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverBreak* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1642_6pin_2048fs_c_1q indicates a TEST FAILED (with missing messages) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific DUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverBreak* response, message reception is terminated and the broken message will be lost. In case the MDUT does not re-transmit the broken message, the MITB will indicate a missing message and TEST FAILED. If the broken message is re-transmitted by the MDUT after receiving the *ReceiverBreak* response, the MITB will not detect any errors.

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Test Name	*mitb_t1642_6pin_2048fs_c_1q*						
Description	2048xFs test with ReceiverBreak responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB generates 48 ReceiverBreak responses on the Control Rx Channel (ChannelAddress 0x0002) of the DUT OS81110 - ReceiverBreak responses generated with a delay of 200 ms between consecutive ReceiverBreaks						
Test Configuration Files	*mitb_t1642_6pin_2048fs_c_1q_cfg_setup.txt* *mitb_t1642_6pin_2048fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…	…	
				…	…	…	
				PC57	0x003E	Unused	
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Disable	5000	500	Enable	Byte Counter	ReceiverBreak	5	100

Table 8-16: mitb_t1642_6pin_2048fs_c_1q

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8.2.14 mitb_t1643_6pin_2048fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting control data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverProtocolError* responses.

After the data transfer is started, the MITB will generate 20 *ReceiverProtocolError* responses on the Control Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverProtocolError* responses are generated with a delay of 100 ms between consecutive *ReceiverProtocolError*.

The MDUT transmitting control messages needs to detect the *ReceiverProtocolError* responses. Following the detection of the *ReceiverProtocolError* the MDUT must stop message transmission following the MediaLB protocol defined in the MediaLB spec. The user needs to verify manually, that the MDUT is properly terminating the message transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverProtocolError* response is signalled properly. The MITB does not provide an indication if the MDUT is handling the *ReceiverProtocolError* as expected.

To verify the MDUT behavior and capture the generated *ReceiverProtocolError* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverProtocolError* responses randomly, it cannot be guaranteed, that the *ReceiverProtocolError* responses always happen at times when the MDUT is transmitting control messages. By that means, it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverProtocolError* responses. It might happen that the *ReceiverProtocolError* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverProtocolError* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverProtocolError* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1643_6pin_2048fs_c_1q indicates a TEST FAILED (with missing messages) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific MDUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverProtocolError* response, message reception is terminated and the broken message will be lost. In case the MDUT does not re-transmit the broken message, the MITB will indicate a missing message and a TEST FAILED. If the broken message is re-transmitted by the MDUT after receiving the *ReceiverProtocolError* response, the MITB will not detect any errors.

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Test Name	*mitb_t1643_6pin_2048fs_c_1q*						
Description	2048xFs test with ReceiverProtocolErr responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB generates 20 ReceiverProtocolError responses on the Control Rx Channel (ChannelAddress 0x0002) of the DUT OS81110 - ReceiverProtocolError responses generated with a delay of 100 ms between consecutive ReceiverProtocolError						
Test Configuration Files	*mitb_t1643_6pin_2048fs_c_1q_cfg_setup.txt* *mitb_t1643_6pin_2048fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…	…	
				…	…	…	
				PC57	0x003E	Unused	
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Disable	5000	500	Enable	Byte Counter	ReceiverProtocolError	5	100

Table 8-17: mitb_t1643_6pin_2048fs_c_1q

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8.2.15 mitb_t1644_6pin_2048fs_c_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is receiving control data and the transmitting device (OS81110 connected to the MDUT) is sending *ControlBreak* commands.

After the data transfer is started, the MITB will transmit 240 *ControlBreak* command on the Control Tx Channel (ChannelAddress 0x0004) of the OS81110. *ControlBreak* commands are generated with a delay of 20 ms between consecutive *ControlBreak*s.

The MDUT receiving control messages needs to detect the *ControlBreak* commands. Following the detection of the *ControlBreak* the MDUT must stop an ongoing message reception. Already received data quadlets are considered to be invalid and should be rejected. The user needs to verify manually, that the MDUT is properly terminating the message reception. Additionally it may be verified if MDUT internally a status indicating the detection of the *ControlBreak* command is signalled properly. The MITB does not provide an indication if the MDUT is handling the *ControlBreak* as expected.

To verify the MDUT behavior and capture the generated *ControlBreak* command generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ControlBreak* commands randomly, it cannot be guaranteed, that the *ControlBreak* command always happen at times when the OS81110 is transmitting control messages. By that means it is not guaranteed, that the MDUT is receiving a message when the *ControlBreak* command is transmitted by the OS81110. Since the MDUT may not receive a message when the *ControlBreak* is present on the MediaLB bus, the *ControlBreak* command may not be detected by the MDUT. In that case the *ControlBreak* commands have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ControlBreak* command by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t1644_6pin_2048fs_c_1q is expected to indicate a TEST PASS. This is the case, because the messages terminated by a *ControlBreak* command are re-transmitted entirely by the OS81110.

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Test Name	*mitb_t1644_6pin_2048fs_c_1q*						
Description	2048xFs test with ControlBreak commands generated by MITB - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 45 Bytes - Throughput 500 msgs/s - MITB transmits 240 ControlBreak commands on the Control Tx Channel (ChannelAddress 0x0004) of the DUT OS81110 - ControlBreak commands generated with a delay of 20 ms between consecutive ControlBreaks						
Test Configuration Files	*mitb_t1644_6pin_2048fs_c_1q_cfg_setup.txt* *mitb_t1644_6pin_2048fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…	…	
				…	…	…	
				PC57	0x003E	Unused	
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	45	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type	TxCmd	Nr. TxCmd	Delay TxCmd (ms)
Disable	5000	500	Enable	Byte Counter	ControlBreak	240	20

Table 8-18: mitb_t1644_6pin_2048fs_c_1q

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8.2.16 mitb_t1650_6pin_3072fs_c_1q

Test Name	*mitb_t1650_6pin_3072fs_c_1q*						
Description	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 14 Bytes - Throughput 250 msgs/s						
Test Configuration Files	*mitb_t1650_6pin_3072fs_c_1q_cfg_setup.txt* *mitb_t1650_6pin_3072fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	3072xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…	…	
				PC57	0x003E	Unused	
				…			
				PC86	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	3072xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	250	Enable	Byte Counter			

Table 8-19: mitb_t1650_6pin_3072fs_c_1q

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8.2.17 mitb_t1651_6pin_3072fs_c_1q

Test Name	*mitb_t1651_6pin_3072fs_c_1q*						
Description	3072xFs test with min/max msg length, max throughput - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 475 msgs/s						
Test Configuration Files	*mitb_t1651_6pin_3072fs_c_1q_cfg_setup.txt* *mitb_t1651_6pin_3072fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	3072xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…			
				PC57	0x003E	Unused	
				…	…	…	
				PC86	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	3072xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Enable	-	6	45	1	1		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	475	Enable	Byte Counter			

Table 8-20: mitb_t1651_6pin_3072fs_c_1q

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8.2.18 mitb_t1660_6pin_4096fs_c_1q

Test Name	*mitb_t1660_6pin_4096fs_c_1q*						
Description	Basic 4096xFs test - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Fixed Message Length 14 Bytes - Throughput 250 msgs/s						
Test Configuration Files	*mitb_t1660_6pin_4096fs_c_1q_cfg_setup.txt* *mitb_t1660_6pin_4096fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	4096xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…	…	…	
				PC57	0x003E	Unused	
				…			
				PC116	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	4096xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	250	Enable	Byte Counter			

Table 8-21: mitb_t1660_6pin_4096fs_c_1q

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8.2.19 mitb_t1661_6pin_4096fs_c_1q

Test Name	***mitb_t1661_6pin_4096fs_c_1q***						
Description	4096xFs test with min/max msg length, max throughput - Concurrent Rx and Tx transfer of MediaLB control data - Blockwidth 2 x 1 quadlet per frame - Variable Message Length - Throughput 475 msgs/s						
Test Configuration Files	*mitb_t1661_6pin_4096fs_c_1q_cfg_setup.txt* *mitb_t1661_6pin_4096fs_c_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	4096xFs	Control	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				…			
				PC57	0x003E	Unused	
				…	…	…	
				PC116	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	4096xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Enable	-	6	45	1	1		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	475	Enable	Byte Counter			

Table 8-22: mitb_t1661_6pin_4096fs_c_1q

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8.3 Asynchronous Tests

The following table provides an overview of available asynchronous data tests.

Overview Asynchronous Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t2310_3pin_256fs_a_1q	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us
mitb_t2320_3pin_512fs_a_1q	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us
mitb_t2321_3pin_512fs_a_7q	512xFs test with 2 x 7q blockwidth - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 7 quadlet per frame - Variable Packet Length - Packet Delay 5200 us
mitb_t2330_3pin_1024fs_a_1q	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us
mitb_t2331_3pin_1024fs_a_15q	1024xFs test with maximum blockwidth - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 1000 us
mitb_t2332_3pin_1024fs_a_5q	1024xFs test with intermediate Blockwidth and min. and max. packet length - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 5 quadlet per frame - Variable Packet Length - Packet Delay 1100 us
mitb_t2333_3pin_1024fs_a_15q	1024xFs test with alternating physical positions for Rx and Tx channels - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 2000 us

Table 8-23: Asynchronous Test Overview (Part 1)

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Overview Asynchronous Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t2334_3pin_1024fs_a_15q	1024xFs test with alternating physical positions for Rx and Tx channels - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 2000 us
mitb_t2335_3pin_1024fs_a_1q	1024xFs test with minimum Packet Delay and ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Variable Packet Length - Packet Delay 5200 us - CA = 0x003A, CA = 0x003E
mitb_t2336_3pin_1024fs_a_5q	1024xFs test with MEP transfer, min. and max. MEP packet length - Concurrent Rx and Tx transfer of MediaLB asynchronous MEP data packets - Blockwidth 2 x 5 quadlet per frame - Variable Packet Length - Packet Delay 2000 us
mitb_t2338_3pin_1024fs_a_1q	1024xFs test with RxBusy Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us
mitb_t2339_3pin_1024fs_a_4q	1024xFs test with RxBreak Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length 500 Bytes - Packet Delay 1500 us
mitb_t23310_3pin_1024fs_a_1q	1024xFs test with RxProtErr Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us
mitb_t23311_3pin_1024fs_a_4q	1024xFs test with Tx Break Command generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length 500 Bytes - Packet Delay 2000 us

Table 8-24: Asynchronous Test Overview (Part 2)

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Overview Asynchronous Tests	
Test Name	**Test Characteristics**
MediaLB 6-pin Tests	
mitb_t2640_6pin_2048fs_a_1q	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 16 Bytes - Packet Delay 2000 us
mitb_t2641_6pin_2048fs_a_27q	2048xFs test with 2 x 27q blockwidth - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 27 quadlet per frame - Variable Packet Length - Packet Delay 2000 us
mitb_t2642_6pin_2048fs_a_5q	2048xFs test with 2 x 5q blockwidth and ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 5 quadlet per frame - Variable Packet Length - Packet Delay 2000 us - CA=0x007E & CA=0x7C
mitb_t2643_6pin_2048fs_a_1q	2048xFs test with RxBusy Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length: 16 Bytes - Packet Delay 2000 us
mitb_t2644_6pin_2048fs_a_4q	2048xFs test with RxBreak Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length: 500 Bytes - Packet Delay 1500 us
mitb_t2645_6pin_2048fs_a_1q	2048xFs test with RxProtocollError Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length: 16 Bytes - Packet Delay 2000 us
mitb_t2646_6pin_2048fs_a_4q	2048xFs test with TxBreak Command generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length: 500 Bytes - Packet Delay 2000 us
mitb_t2650_6pin_3072fs_a_1q	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 32 Bytes - Packet Delay 2000 us

Table 8-25: Asynchronous Test Overview (Part 3)

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Overview Asynchronous Tests	
Test Name	**Test Characteristics**
MediaLB 6-pin Tests	
mitb_t2651_6pin_3072fs_a_27q	3072xFs test with min/max packet length, max bandwidth - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 27 quadlet per frame - Varied Packet Length - Packet Delay 6000 us
mitb_t2660_6pin_4096fs_a_1q	Basic 4096xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 32 Bytes - Packet Delay 2000 us

Table 8-26: Asynchronous Test Overview (Part 4)

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8.3.1 mitb_t2310_3pin_256fs_a_1q

Test Name	*mitb_t2310_3pin_256fs_a_1q*						
Test Characteristic	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2310_3pin_256fs_a_1q_cfg_setup.txt* *mitb_t2310_3pin_256fs_a_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	256xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…		
				PC7	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	256xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	2000	Enable	Byte Counter			

Table 8-27: mitb_t2310_3pin_256fs_a_1q

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8.3.2 mitb_t2320_3pin_512fs_a_1q

Test Name	*mitb_t2320_3pin_512fs_a_1q*						
Test Characteristic	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2320_3pin_512fs_a_1q_cfg_setup.txt* *mitb_t2320_3pin_512fs_a_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	512xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…		
				PC15	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	512xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	2000	Enable	Byte Counter			

Table 8-28: mitb_t2320_3pin_512fs_a_1q

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8.3.3 mitb_t2321_3pin_512fs_a_7q

Test Name	*mitb_t2321_3pin_512fs_a_7q*						
Test Characteristic	512xFs test with 2 x 7q blockwidth - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 7 quadlet per frame - Variable Packet Length - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2321_3pin_512fs_a_7q_cfg_setup.txt* *mitb_t2321_3pin_512fs_a_7q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	512xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				…	…	…	
				PC7	0x0006	Async Rx	
				PC8	0x0008	Async Tx	
				…	…	…	
				PC14	0x0008	Async Tx	
				PC15	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	512xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	7	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	6	1014	1	3		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	5200	Enable	Random			

Table 8-29: mitb_t2321_3pin_512fs_a_7q

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8.3.4 mitb_t2330_3pin_1024fs_a_1q

Test Name	***mitb_t2330_3pin_1024fs_a_1q***						
Test Characteristic	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2330_3pin_1024fs_a_1q_cfg_setup.txt* *mitb_t2330_3pin_1024fs_a_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…	…	
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Enable	5000	2000	Enable	Byte Counter			

Table 8-30: mitb_t2330_3pin_1024fs_a_1q

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8.3.5 mitb_t2331_3pin_1024fs_a_15q

Test Name	*mitb_t2331_3pin_1024fs_a_15q*						
Test Characteristic	1024xFs test with 2 x 15q blockwidth - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2331_3pin_1024fs_a_15q_cfg_setup.txt* *mitb_t2331_3pin_1024fs_a_15q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0002	Async Rx	
				…	…	…	
				PC15	0x0002	Async Rx	
				PC16	0x0004	Async Tx	
				…	…	…	
				PC30	0x0004	Async Tx	
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0002	0x0004	15	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	54	1014	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	1000	Enable	Random			

Table 8-31: mitb_t2331_3pin_1024fs_a_15q

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8.3.6 mitb_t2332_3pin_1024fs_a_5q

Test Name	*mitb_t2332_3pin_1024fs_a_5q*						
Test Characteristic	1024xFs test with intermediate Blockwidth and min. and max. packet length - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 5 quadlet per frame - Variable Packet Length (6..1014 byte) - Packet Delay 1000 us						
Test Configuration Files	*mitb_t2332_3pin_1024fs_a_5q_cfg_setup.txt* *mitb_t2332_3pin_1024fs_a_5q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0002	Async Rx	
				…	…	…	
				PC5	0x0002	Async Rx	
				PC6	0x0004	Async Tx	
				…	…	…	
				PC10	0x0004	Async Tx	
				..	..		
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0002	0x0004	5	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	118	1014	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	1100	Enable	Byte Counter			

Table 8-32: mitb_t2332_3pin_1024fs_a_5q

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8.3.7 mitb_t2333_3pin_1024fs_a_15q

Test Name	*mitb_t2333_3pin_1024fs_a_15q*		
Test Characteristic	1024xFs test with alternating physical positions for Rx and Tx channels - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 2000 us		
Test Configuration Files	*mitb_t2333_3pin_1024fs_a_15q_cfg_setup.txt* *mitb_t2333_3pin_1024fs_a_15q_cfg_start.txt*	Manual setup of test via GUI possible?	No

DUT MediaLB Configuration						
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer
Device	3-Pin	1024xFs	Async	PC0	0x01FE	
				PC1	0x0002	Async Rx
				PC2	0x0004	Async Tx
				PC3	0x0002	Async Rx
				PC4	0x0002	Async Rx
				PC5	0x0004	Async Tx
				PC6	0x0004	Async Tx
				PC7	0x0002	Async Rx
				PC8	0x0002	Async Rx
				PC9	0x0002	Async Rx
				PC10	0x0004	Async Tx
				PC11	0x0004	Async Tx
				PC12	0x0004	Async Tx
				PC13	0x0002	Async Rx
				PC14	0x0002	Async Rx
				PC15	0x0002	Async Rx
				PC16	0x0002	Async Rx
				PC17	0x0004	Async Tx
				PC18	0x0004	Async Tx
				PC19	0x0004	Async Tx
				PC20	0x0004	Async Tx
				PC21	0x0002	Async Rx
				PC22	0x0002	Async Rx
				PC23	0x0002	Async Rx
				PC24	0x0002	Async Rx
				PC25	0x0002	Async Rx
				PC26	0x0004	Async Tx
				PC27	0x0004	Async Tx
				PC28	0x0004	Async Tx
				PC29	0x0004	Async Tx
				PC30	0x0004	Async Tx
				PC31	0x0000	

Table 8-33: mitb_t2333_3pin_1024fs_a_15q (Part 1)

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Test Name	*mitb_t2333_3pin_1024fs_a_15q*						
Test Characteristic	1024xFs test with alternating physical positions for Rx and Tx channels - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2333_3pin_1024fs_a_15q_cfg_setup.txt* *mitb_t2333_3pin_1024fs_a_15q_cfg_start.txt*				Manual setup of test via GUI possible?		No
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0002	0x0004	15	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	7	1014	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	2000	Enable	Random			

Table 8-34: mitb_t2333_3pin_1024fs_a_15q (Part 2)

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8.3.8 mitb_t2334_3pin_1024fs_a_15q

Test Name	*mitb_t2334_3pin_1024fs_a_15q*		
Test Characteristic	1024xFs test with alternating physical positions for Rx and Tx channels - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 2000 us		
Test Configuration Files	*mitb_t2334_3pin_1024fs_a_15q_cfg_setup.txt* *mitb_t2334_3pin_1024fs_a_15q_cfg_start.txt*	Manual setup of test via GUI possible?	No

DUT MediaLB Configuration						
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer
Device	3-Pin	1024xFs	Async	PC0	0x01FE	
				PC1	0x0004	Async Tx
				PC2	0x0002	Async Rx
				PC3	0x0004	Async Tx
				PC4	0x0004	Async Tx
				PC5	0x0002	Async Rx
				PC6	0x0002	Async Rx
				PC7	0x0004	Async Tx
				PC8	0x0004	Async Tx
				PC9	0x0004	Async Tx
				PC10	0x0002	Async Rx
				PC11	0x0002	Async Rx
				PC12	0x0002	Async Rx
				PC13	0x0004	Async Tx
				PC14	0x0004	Async Tx
				PC15	0x0004	Async Tx
				PC16	0x0004	Async Tx
				PC17	0x0002	Async Rx
				PC18	0x0002	Async Rx
				PC19	0x0002	Async Rx
				PC20	0x0002	Async Rx
				PC21	0x0004	Async Tx
				PC22	0x0004	Async Tx
				PC23	0x0004	Async Tx
				PC24	0x0004	Async Tx
				PC25	0x0004	Async Tx
				PC26	0x0002	Async Rx
				PC27	0x0002	Async Rx
				PC28	0x0002	Async Rx
				PC29	0x0002	Async Rx
				PC30	0x0002	Async Rx
				PC31	0x0000	

Table 8-35: mitb_t2334_3pin_1024fs_a_15q (Part 1)

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Test Name	*mitb_t2334_3pin_1024fs_a_15q*						
Test Characteristic	1024xFs test with alternating physical positions for Rx and Tx channels - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 15 quadlet per frame - Variable Packet Length - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2334_3pin_1024fs_a_15q_cfg_setup.txt* *mitb_t2334_3pin_1024fs_a_15q_cfg_start.txt*				Manual setup of test via GUI possible?		No
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0002	0x0004	15	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	7	1014	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	2000	Enable	Random			

Table 8-36: mitb_t2334_3pin_1024fs_a_15q (Part 2)

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8.3.9 mitb_t2335_3pin_1024fs_a_1q

Test Name	*mitb_t2335_3pin_1024fs_a_1q*						
Test Characteristic	1024xFs test with minimum Packet Delay and ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Variable Packet Length - Packet Delay 1000 us - CA = 0x003A, CA = 0x0038						
Test Configuration Files	*mitb_t2335_3pin_1024fs_a_1q_cfg_setup.txt* *mitb_t2335_3pin_1024fs_a_1q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x003A	Async Rx	
				PC2	0x0038	Async Tx	
				…	…	…	
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x003A	0x0038	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	6	1014	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	5200	Enable	Byte Counter			

Table 8-37: mitb_t2335_3pin_1024fs_a_1q

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8.3.10 mitb_t2336_3pin_1024fs_a_5q

Test Name	*mitb_t2336_3pin_1024fs_a_5q*						
Test Characteristic	1024xFs test with MEP transfer - Concurrent Rx and Tx transfer of MediaLB asynchronous MEP data packets - Blockwidth 2 x 5 quadlet per frame - Variable Packet Length - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2336_3pin_1024fs_a_5q_cfg_setup.txt* *mitb_t2336_3pin_1024fs_a_5q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0004	Async Rx	
				…	…	…	
				PC5	0x0004	Async Rx	
				PC6	0x0002	Async Tx	
				…	…	…	
				PC10	0x0002	Async Tx	
				..	..		
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0004	0x0002	5	Enable	0x111111| 222222	0x333333| 444444		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	6	1506	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	2000	Enable	Byte Counter			

Table 8-38: mitb_t2336_3pin_1024fs_a_5q

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8.3.11 mitb_t2338_3pin_1024fs_a_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting Async data and the receiving device (OS81110 connected to the MDUT) is responding with ReceiverBusy responses.

After the data transfer is started, the MITB will generate a series of 20 consecutive ReceiverBusy response periods on the Async Rx Channel (ChannelAddress 0x0008) of the OS81110. During each period, the OS81110 generates ReceiverBusy responses in every frame on the Async Rx Channel for approximately 2 ms. After a delay of 110 ms, at which the OS81110 is able to receive data, indicated by ReceiverReady responses, the next ReceiverBusy period starts.

The ReceiverBusy responses indicate that the OS81110 connected to the MDUT is not able to receive data. The ReceiverBusy responses need to be detected by the MDUT, and transmitted data quadlets acknowledged by a ReceiverBusy response must be repeatedly transmitted until a ReceiverReady response is detected. The user must verify this behavior manually. The MITB does not provide an indication if the ReceiverBusy is handled properly by the MDUT.

To verify the MDUT behavior and capture the generated ReceiverBusy responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating ReceiverBusy responses randomly, it cannot be guaranteed, that the ReceiverBusy responses always happen at times when the MDUT is transmitting Async messages. By that means it is not guaranteed, that MediaLB commands 0x20, 0x22 and 0x24 transmitted by the MDUT are acknowledged by ReceiverBusy responses. It might happen that the ReceiverBusy responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the ReceiverBusy responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the ReceiverBusy response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t2338_3pin_1024fs_a_1q indicates in most cases a TEST PASS in the MITB GUI. This behavior relates to the length of the ReceiverBusy periods as well as to the MDUT packet buffer size.

In some cases the MITB test case mitb_t2338_3pin_1024fs_a_1q might indicate a TEST FAILED (with missing messages) in the MITB GUI. This behavior is expected and is related to the nature of the MOST network and the OS81110 as well as to the packet buffer size on the MDUT.

During the ReceiverBusy periods the OS81110 will not receive data from the MDUT via MediaLB. Since loop-back application of the MDUT cannot transmit any data, it also will only be able to receive a certain amount of new packets from the OS81110 via MediaLB and the MITB respectively. Large packet buffers allow the MDUT to keep receiving more packets, where as with small packet buffers, the MDUT will stop receiving data quite fast. This again results in the OS81110 holding of messages received via MOST from the MITB platform. Depending on how long the ReceiverBusy period lasts and how deep the MDUT packet buffers are, the OS81110 buffers will run full and packets transmitted from MITB platform to OS81110 via MOST will get lost on the MOST network. There is no such thing as a ReceiverBusy response on MOST. Because of this, no feedback from the OS81110 connected to the DUT is passed to the OS81110 on the MITB platform, indicating the buffer full condition of the DUT OS81110 and the MITB keeps transmitting packets, which may get lost.

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Test Name	*mitb_t2338_3pin_1024fs_a_1q*						
Test Characteristic	1024xFs test with ReceiverBusy responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us - MITB generates series of 20 consecutive ReceiverBusy response periods on Async Rx Channel (ChannelAddress 0x0008) of the MDUT OS81110 - During each period, ReceiverBusy responses generated in every frame for approximately 2 ms, After delay of 110 ms, next ReceiverBusy period starts						
Test Configuration Files	*mitb_t2338_3pin_1024fs_a_1q_cfg_setup.txt* *mitb_t2338_3pin_1024fs_a_1q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				...	...	...	
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Enable	5000	2000	Enable	Byte Counter	ReceiverBusy	20	110

Table 8-39: mitb_t2338_3pin_1024fs_a_1q

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8.3.12 mitb_t2339_3pin_1024fs_a_4q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting async data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverBreak* responses.

After the data transfer is started, the MITB will generate 32 *ReceiverBreak* responses on the Async Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverBreak* responses are generated with a delay of 5 ms between consecutive *ReceiverBreak*s.

The MDUT transmitting async packets needs to detect the *ReceiverBreak* responses. Following the detection of the *ReceiverBreak* the MDUT must stop packet transmission. The user needs to verify manually, that the MDUT is properly terminating the packet transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverBreak* response is signalled. The MITB does not provide an indication if the MDUT is handling the *ReceiverBreak*s as expected.

To verify the MDUT behavior and capture the generated *ReceiverBreak* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverBreak* responses randomly, it cannot be guaranteed, that the *ReceiverBreak* responses always happen at times when the MDUT is transmitting async packets. By that means, it is not guaranteed, that MediaLB commands 0x20, 0x22 and 0x24 transmitted by the MDUT are acknowledged by *ReceiverBreak* responses. It might happen that the *ReceiverBreak* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverBreak* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverBreak* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t2339_3pin_1024fs_c_4q indicates a TEST FAILED (with missing packets) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific DUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverBreak* response, packet reception is terminated and the broken packet will be lost. In case the MDUT does not re-transmit the broken packet, the MITB will indicate a missing packet and TEST FAILED. If the broken packet is re-transmitted by the MDUT after receiving the *ReceiverBreak* response, the MITB will not detect any errors.

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Test Name	*mitb_t2339_3pin_1024fs_a_4q*						
Test Characteristic	1024xFs test with ReceiverBreak responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length 500 Bytes - Packet Delay 1500 us - MITB generates 32 ReceiverBreak responses on the Async Rx Channel (ChannelAddress 0x0008) of the MDUT OS81110 - ReceiverBreak responses generated with a delay of 5 ms between consecutive ReceiverBreaks						
Test Configuration Files	*mitb_t2339_3pin_1024fs_a_4q_cfg_setup.txt* *mitb_t2339_3pin_1024fs_a_4q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0006	Async Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0006	Async Rx	
				PC5	0x0008	Async Tx	
				PC6	0x0008	Async Tx	
				PC7	0x0008	Async Tx	
				PC8	0x0008	Async Tx	
				…	…	…	
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	4	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	500	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Enable	5000	1500	Enable	Byte Counter	ReceiverBreak	32	5

Table 8-40: mitb_t2339_3pin_1024fs_a_4q

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8.3.13 mitb_t23310_3pin_1024fs_a_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting async data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverProtocolError* responses.

After the data transfer is started, the MITB will generate 32 *ReceiverProtocolError* responses on the Async Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverProtocolError* responses are generated with a delay of 100 ms between consecutive *ReceiverProtocolError*.

The MDUT transmitting async packets needs to detect the *ReceiverProtocolError* responses. Following the detection of the *ReceiverProtocolError* the MDUT must stop packet transmission following the MediaLB protocol defined in the MediaLB spec. The user needs to verify manually, that the MDUT is properly terminating the packet transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverProtocolError* response is signalled properly. The MITB does not provide an indication if the MDUT is handling the *ReceiverProtocolError* as expected.

To verify the MDUT behavior and capture the generated *ReceiverProtocolError* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverProtocolError* responses randomly, it cannot be guaranteed, that the *ReceiverProtocolError* responses always happen at times when the MDUT is transmitting async packets. By that means, it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverProtocolError* responses. It might happen that the *ReceiverProtocolError* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverProtocolError* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverProtocolError* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t23310_3pin_1024fs_c_1q indicates a TEST FAILED (with missing packets) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific MDUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverProtocolError* response, packet reception is terminated and the broken packet will be lost. In case the MDUT does not re-transmit the broken packet, the MITB will indicate a missing packet and a TEST FAILED. If the broken packet is re-transmitted by the MDUT after receiving the *ReceiverProtocolError* response, the MITB will not detect any errors.

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Test Name	*mitb_t23310_3pin_1024fs_a_1q*						
Test Characteristic	1024xFs test with ReceoverProtocolError responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us - MITB generates 32 ReceiverProtocolError responses on the Async Rx Channel (ChannelAddress 0x0008) of the DUT OS81110 - ReceiverProtocolError responses generated with a delay of 100 ms between consecutive ReceiverProtocolError						
Test Configuration Files	*mitb_t23310_3pin_1024fs_a_1q_cfg_setup.txt* *mitb_t23310_3pin_1024fs_a_1q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…	…	
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Enable	5000	2000	Enable	Byte Counter	ReceiverProtocolError	32	100

Table 8-41: mitb_t23310_3pin_1024fs_a_1q

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8.3.14 mitb_t23311_3pin_1024fs_a_4q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is receiving async data and the transmitting device (OS81110 connected to the MDUT) is sending *AsyncBreak* commands.

After the data transfer is started, the MITB will transmit 16 *AsyncBreak* command on the Async Tx Channel (ChannelAddress 0x0004) of the OS81110. *AsyncBreak* commands are generated with a delay of 5 ms between consecutive *AsyncBreak*s.

The MDUT receiving async packets needs to detect the *AsyncBreak* commands. Following the detection of the *AsyncBreak* the MDUT must stop an ongoing packet reception. Already received data quadlets are considered to be invalid and should be rejected. The user needs to verify manually, that the MDUT is properly terminating the packet reception. Additionally it may be verified if MDUT internally a status indicating the detection of the *AsyncBreak* command is signalled properly. The MITB does not provide an indication if the MDUT is handling the *AsyncBreak* as expected.

To verify the MDUT behavior and capture the generated *AsyncBreak* command generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *AsyncBreak* commands randomly, it cannot be guaranteed, that the *AsyncBreak* command always happen at times when the OS81110 is transmitting async packets. By that means it is not guaranteed, that the MDUT is receiving a packet when the *AsyncBreak* command is transmitted by the OS81110. Since the MDUT may not receive a packet when the *AsyncBreak* is present on the MediaLB bus, the *AsyncBreak* command may not be detected by the MDUT. In that case the *AsyncBreak* commands have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *AsyncBreak* command by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t23311_3pin_1024fs_c_4q is expected to indicate a TEST PASS. This is the case, because the packets terminated by an *AsyncBreak* command are re-transmitted entirely by the OS81110.

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Test Name	*mitb_t23311_3pin_1024fs_a_4q*						
Test Characteristic	1024xFs test with AsyncBreak commands generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length 500 Bytes - Packet Delay 2000 us - MITB transmits 32 AsyncBreak commands on the Async Tx Channel (ChannelAddress 0x0006) of the MDUT OS81110 - AsyncBreak commands generated with a delay of 4 ms between consecutive AsyncBreaks						
Test Configuration Files	*mitb_t23311_3pin_1024fs_a_4q_cfg_setup.txt* *mitb_t23311_3pin_1024fs_a_4q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0006	Async Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0006	Async Rx	
				PC5	0x0008	Async Tx	
				PC6	0x0008	Async Tx	
				PC7	0x0008	Async Tx	
				PC8	0x0008	Async Tx	
				…	…	…	
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	4	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	500	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	TxCmd	Nr. TxCmd	Delay TxCmd (ms)
Enable	5000	2000	Enable	Byte Counter	AsyncBreak	32	4

Table 8-42: mitb_t23311_3pin_1024fs_a_4q

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8.3.15 mitb_t2640_6pin_2048fs_a_1q

Test Name	***mitb_t2640_6pin_2048fs_a_1q***						
Test Characteristic	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2640_6pin_2048fs_a_1q_cfg_setup.txt* *mitb_t2640_6pin_2048fs_a_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…	…	
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	16	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Enable	5000	2000	Enable	Byte Counter			

Table 8-43: mitb_t2640_6pin_2048fs_a_1q

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8.3.16 mitb_t2641_6pin_2048fs_a_27q

Test Name	*mitb_t2641_6pin_2048fs_a_27q*						
Test Characteristic	2048xFs test with 2 x 27q blockwidth - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 27 quadlet per frame - Variable Packet Length - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2641_6pin_2048fs_a_27q_cfg_setup.txt* *mitb_t2641_6pin_2048fs_a_27q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				…	…	…	
				PC27	0x0006	Async Rx	
				PC28	0x0008	Async Tx	
				…	…	…	
				PC54	0x0008	Async Tx	
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	27	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	6	1014	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	2000	Enable	Random			

Table 8-44: mitb_t2641_6pin_2048fs_a_27q

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8.3.17 mitb_t2642_6pin_2048fs_a_5q

Test Name	*mitb_t2642_6pin_2048fs_a_5q*						
Test Characteristic	2048xFs test with 2 x 5q blockwidth and ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 5 quadlet per frame - Variable Packet Length - Packet Delay 2000 us - CA=0x007E & CA=0x7C						
Test Configuration Files	*mitb_t2642_6pin_2048fs_a_5q_cfg_setup.txt* *mitb_t2642_6pin_2048fs_a_5q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Async	PC0	0x01FE		
				PC1	0x007C	Async Rx	
				…	…	…	
				PC5	0x007C	Async Rx	
				PC6	0x007E	Async Tx	
				…	…	…	
				PC11	0x0008	Async Tx	
				…	…		
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x007C	0x007E	5	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	22	1014	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	2000	Enable	Byte Counter			

Table 8-45: mitb_t2642_6pin_2048fs_a_5q

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8.3.18 mitb_t2643_6pin_2048fs_a_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting Async data and the receiving device (OS81110 connected to the MDUT) is responding with ReceiverBusy responses.

After the data transfer is started, the MITB will generate a series of 20 consecutive ReceiverBusy response periods on the Async Rx Channel (ChannelAddress 0x0008) of the OS81110. During each period, the OS81110 generates ReceiverBusy responses in every frame on the Async Rx Channel for approximately 2 ms. After a delay of 110 ms, at which the OS81110 is able to receive data, indicated by ReceiverReady responses, the next ReceiverBusy period starts.

The ReceiverBusy responses indicate that the OS81110 connected to the MDUT is not able to receive data. The ReceiverBusy responses need to be detected by the MDUT, and transmitted data quadlets acknowledged by a ReceiverBusy response must be repeatedly transmitted until a ReceiverReady response is detected. The user must verify this behavior manually. The MITB does not provide an indication if the ReceiverBusy is handled properly by the MDUT.

To verify the MDUT behavior and capture the generated ReceiverBusy responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating ReceiverBusy responses randomly, it cannot be guaranteed, that the ReceiverBusy responses always happen at times when the MDUT is transmitting Async messages. By that means it is not guaranteed, that MediaLB commands 0x20, 0x22 and 0x24 transmitted by the MDUT are acknowledged by ReceiverBusy responses. It might happen that the ReceiverBusy responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the ReceiverBusy responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the ReceiverBusy response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t2643_6pin_2048fs_a_1q indicates in most cases a TEST PASS in the MITB GUI. This behavior relates to the length of the ReceiverBusy periods as well as to the MDUT packet buffer size.

In some cases the MITB test case mitb_t2643_6pin_2048fs_a_1q might indicate a TEST FAILED (with missing messages) in the MITB GUI. This behavior is expected and is related to the nature of the MOST network and the OS81110 as well as to the packet buffer size on the MDUT.

During the ReceiverBusy periods the OS81110 will not receive data from the MDUT via MediaLB. Since loop-back application of the MDUT cannot transmit any data, it also will only be able to receive a certain amount of new packets from the OS81110 via MediaLB and the MITB respectively. Large packet buffers allow the MDUT to keep receiving more packets, where as with small packet buffers, the MDUT will stop receiving data quite fast. This again results in the OS81110 holding of messages received via MOST from the MITB platform. Depending on how long the ReceiverBusy period lasts and how deep the MDUT packet buffers are, the OS81110 buffers will run full and packets transmitted from MITB platform to OS81110 via MOST will get lost on the MOST network. There is no such thing as a ReceiverBusy response on MOST. Because of this, no feedback from the OS81110 connected to the DUT is passed to the OS81110 on the MITB platform, indicating the buffer full condition of the DUT OS81110 and the MITB keeps transmitting packets, which may get lost.

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Test Name	*mitb_t2643_6pin_2048fs_a_1q*						
Test Characteristic	2048xFs test with ReceiverBusy Responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us - MITB generates series of 20 consecutive ReceiverBusy response periods on Async Rx Channel (ChannelAddress 0x0008) of the MDUT OS81110 - During each period, ReceiverBusy responses generated in every frame for approximately 2 ms, After delay of 110 ms, next ReceiverBusy period starts						
Test Configuration Files	*mitb_t2643_6pin_2048fs_a_1q_cfg_setup.txt* *mitb_t2643_6pin_2048fs_a_1q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…	…	
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	16	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Enable	5000	2000	Enable	Byte Counter	ReceiverBusy	20	110

Table 8-46: mitb_t2643_6pin_2048fs_a_1q

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8.3.19 mitb_t2644_6pin_2048fs_a_4q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting async data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverBreak* responses.

After the data transfer is started, the MITB will generate 32 *ReceiverBreak* responses on the Async Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverBreak* responses are generated with a delay of 5 ms between consecutive *ReceiverBreak*s.

The MDUT transmitting async packets needs to detect the *ReceiverBreak* responses. Following the detection of the *ReceiverBreak* the MDUT must stop packet transmission. The user needs to verify manually, that the MDUT is properly terminating the packet transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverBreak* response is signalled. The MITB does not provide an indication if the MDUT is handling the *ReceiverBreak*s as expected.

To verify the MDUT behavior and capture the generated *ReceiverBreak* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverBreak* responses randomly, it cannot be guaranteed, that the *ReceiverBreak* responses always happen at times when the MDUT is transmitting async packets. By that means, it is not guaranteed, that MediaLB commands 0x20, 0x22 and 0x24 transmitted by the MDUT are acknowledged by *ReceiverBreak* responses. It might happen that the *ReceiverBreak* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverBreak* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverBreak* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t2644_6pin_2048fs_c_4q indicates a TEST FAILED (with missing packets) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific DUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverBreak* response, packet reception is terminated and the broken packet will be lost. In case the MDUT does not re-transmit the broken packet, the MITB will indicate a missing packet and TEST FAILED. If the broken packet is re-transmitted by the MDUT after receiving the *ReceiverBreak* response, the MITB will not detect any errors.

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Test Name	*mitb_t2644_6pin_2048fs_a_4q*		
Test Characteristic	2048xFs test with ReceiverBreak responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length 500 Bytes - Packet Delay 1500 us - MITB generates 32 ReceiverBreak responses on the Async Rx Channel (ChannelAddress 0x0008) of the MDUT OS81110 - ReceiverBreak responses generated with a delay of 5 ms between consecutive ReceiverBreaks		
Test Configuration Files	*mitb_t2644_6pin_2048fs_a_4q_cfg_setup.txt* *mitb_t2644_6pin_2048fs_a_4q_cfg_start.txt*	Manual setup of test via GUI possible?	YES

DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0006	Async Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0006	Async Rx	
				PC5	0x0008	Async Tx	
				PC6	0x0008	Async Tx	
				PC7	0x0008	Async Tx	
				PC8	0x0008	Async Tx	
				…	…	…	
				PC57	0x0000		

GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	4	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	500	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Enable	5000	1500	Enable	Byte Counter	ReceiverBreak	32	5

Table 8-47: mitb_t2644_6pin_2048fs_a_4q

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8.3.20 mitb_t2645_6pin_2048fs_a_1q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is transmitting async data and the receiving device (OS81110 connected to the MDUT) is responding with *ReceiverProtocolError* responses.

After the data transfer is started, the MITB will generate 32 *ReceiverProtocolError* responses on the Async Rx Channel (ChannelAddress 0x0002) of the OS81110. *ReceiverProtocolError* responses are generated with a delay of 100 ms between consecutive *ReceiverProtocolError*.

The MDUT transmitting async packets needs to detect the *ReceiverProtocolError* responses. Following the detection of the *ReceiverProtocolError* the MDUT must stop packet transmission following the MediaLB protocol defined in the MediaLB spec. The user needs to verify manually, that the MDUT is properly terminating the packet transmission. Additionally it may be verified if MDUT internally a status indicating the detection of the *ReceiverProtocolError* response is signalled properly. The MITB does not provide an indication if the MDUT is handling the *ReceiverProtocolError* as expected.

To verify the MDUT behavior and capture the generated *ReceiverProtocolError* responses generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *ReceiverProtocolError* responses randomly, it cannot be guaranteed, that the *ReceiverProtocolError* responses always happen at times when the MDUT is transmitting async packets. By that means, it is not guaranteed, that MediaLB commands 0x30, 0x32 and 0x34 transmitted by the MDUT are acknowledged by *ReceiverProtocolError* responses. It might happen that the *ReceiverProtocolError* responses are present on the bus when NoData commands are transmitted by the MDUT. In that case the *ReceiverProtocolError* responses have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *ReceiverProtocolError* response by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t2645_6pin_2048fs_c_1q indicates a TEST FAILED (with missing packets) in the MITB GUI for most cases. This behavior is expected and entirely depends on the customer specific MDUT system re-transmission mechanisms.

If the OS81110 generates a *ReceiverProtocolError* response, packet reception is terminated and the broken packet will be lost. In case the MDUT does not re-transmit the broken packet, the MITB will indicate a missing packet and a TEST FAILED. If the broken packet is re-transmitted by the MDUT after receiving the *ReceiverProtocolError* response, the MITB will not detect any errors.

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Test Name	*mitb_t2645_6pin_2048fs_a_1q*						
Test Characteristic	2048xFs test with ReceiverProtocolError responses generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 14 Bytes - Packet Delay 2000 us - MITB generates 32 ReceiverProtocolError responses on the Async Rx Channel (ChannelAddress 0x0008) of the DUT OS81110 - ReceiverProtocolError responses generated with a delay of 100 ms between consecutive ReceiverProtocolError						
Test Configuration Files	*mitb_t2645_6pin_2048fs_a_1q_cfg_setup.txt* *mitb_t2645_6pin_2048fs_a_1q_cfg_start.txt*			Manual setup of test via GUI possible?		YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…	…	
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	16	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	RxResp	Nr. RxResp	Delay RxResp (ms)
Enable	5000	2000	Enable	Byte Counter	ReceiverProtocolError	32	100

Table 8-48: mitb_t2645_6pin_2048fs_a_1q

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8.3.21 mitb_t2646_6pin_2048fs_a_4q

The purpose of this test is to verify the correct behavior of the MediaLB DUT in case it is receiving async data and the transmitting device (OS81110 connected to the MDUT) is sending *AsyncBreak* commands.

After the data transfer is started, the MITB will transmit 16 *AsyncBreak* command on the Async Tx Channel (ChannelAddress 0x0004) of the OS81110. *AsyncBreak* commands are generated with a delay of 5 ms between consecutive *AsyncBreak*s.

The MDUT receiving async packets needs to detect the *AsyncBreak* commands. Following the detection of the *AsyncBreak* the MDUT must stop an ongoing packet reception. Already received data quadlets are considered to be invalid and should be rejected. The user needs to verify manually, that the MDUT is properly terminating the packet reception. Additionally it may be verified if MDUT internally a status indicating the detection of the *AsyncBreak* command is signalled properly. The MITB does not provide an indication if the MDUT is handling the *AsyncBreak* as expected.

To verify the MDUT behavior and capture the generated *AsyncBreak* command generated by the MITB, it is required to trace the MediaLB data transfer, e.g. with a MediaLB Analyzer.

Since the OS81110 is generating *AsyncBreak* commands randomly, it cannot be guaranteed, that the *AsyncBreak* command always happen at times when the OS81110 is transmitting async packets. By that means it is not guaranteed, that the MDUT is receiving a packet when the *AsyncBreak* command is transmitted by the OS81110. Since the MDUT may not receive a packet when the *AsyncBreak* is present on the MediaLB bus, the *AsyncBreak* command may not be detected by the MDUT. In that case the *AsyncBreak* commands have no effect on the behavior of the MDUT. To still be able to test the proper handling of the *AsyncBreak* command by the MDUT, the test could be executed by configuring the MITB GUI manually with e.g. user specific delay parameters.

The MITB test case mitb_t23311_3pin_1024fs_c_4q is expected to indicate a TEST PASS. This is the case, because the packets terminated by an *AsyncBreak* command are re-transmitted entirely by the OS81110.

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Test Name	*mitb_t2646_6pin_2048fs_a_4q*						
Test Characteristic	2048xFs test with AsyncBreak commands generated by MITB - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 4 quadlet per frame - Fixed Packet Length 500 Bytes - Packet Delay 2000 us - MITB transmits 32 AsyncBreak commands on the Async Tx Channel (ChannelAddress 0x0006) of the MDUT OS81110 - AsyncBreak commands generated with a delay of 4 ms between consecutive AsyncBreaks						
Test Configuration Files	*mitb_t2646_6pin_2048fs_a_4q_cfg_setup.txt* *mitb_t2646_6pin_2048fs_a_4q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0006	Async Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0006	Async Rx	
				PC5	0x0008	Async Tx	
				PC6	0x0008	Async Tx	
				PC7	0x0008	Async Tx	
				PC8	0x0008	Async Tx	
				…	…	…	
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	4	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	500	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type	TxCmd	Nr. TxCmd	Delay TxCmd (ms)
Enable	5000	2000	Enable	Byte Counter	AsyncBreak	32	4

Table 8-49: mitb_t2646_6pin_2048fs_a_4q

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8.3.22 mitb_t2650_6pin_3072fs_a_1q

Test Name	*mitb_t2650_6pin_3072fs_a_1q*						
Test Characteristic	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 32 Bytes - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2650_6pin_3072fs_a_1q_cfg_setup.txt* *mitb_t2650_6pin_3072fs_a_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	3072xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…	…	
				PC86	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	3072xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	32	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Enable	5000	2000	Enable	Byte Counter			

Table 8-50: mitb_t2650_6pin_3072fs_a_1q

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8.3.23 mitb_t2651_6pin_3072fs_a_27q

<table>
<tr><td>Test Name</td><td colspan="7">mitb_t2651_6pin_3072fs_a_27q</td></tr>
<tr><td>Test Characteristic</td><td colspan="7">2048xFs test with 2 x 27q blockwidth
- Concurrent Rx and Tx transfer of MediaLB asynchronous data
- Blockwidth 2 x 27 quadlet per frame
- Variable Packet Length
- Packet Delay 6000 us</td></tr>
<tr><td>Test Configuration Files</td><td colspan="3">mitb_t2651_6pin_3072fs_a_27q_cfg_setup.txt
mitb_t2651_6pin_3072fs_a_27q_cfg_start.txt</td><td colspan="2">Manual setup of test via GUI possible?</td><td colspan="2">YES</td></tr>
<tr><td colspan="8">DUT MediaLB Configuration</td></tr>
<tr><td>Port Mode</td><td>Interface Mode</td><td>Clock Speed</td><td>Transferred Data Type</td><td>Physical Channel</td><td>Channel Address</td><td colspan="2">Allocated Transfer</td></tr>
<tr><td rowspan="11">Device</td><td rowspan="11">6-Pin</td><td rowspan="11">3072xFs</td><td rowspan="11">Async</td><td>PC0</td><td>0x01FE</td><td colspan="2"></td></tr>
<tr><td>PC1</td><td>0x0006</td><td colspan="2">Async Rx</td></tr>
<tr><td>…</td><td>…</td><td colspan="2">…</td></tr>
<tr><td>PC27</td><td>0x0006</td><td colspan="2">Async Rx</td></tr>
<tr><td>PC28</td><td>0x0008</td><td colspan="2">Async Tx</td></tr>
<tr><td>…</td><td>…</td><td colspan="2">…</td></tr>
<tr><td>PC54</td><td>0x0008</td><td colspan="2">Async Tx</td></tr>
<tr><td>…</td><td>…</td><td colspan="2">…</td></tr>
<tr><td>PC86</td><td>0x0000</td><td colspan="2"></td></tr>
<tr><td colspan="8">GUI Configuration</td></tr>
<tr><td colspan="8">Configuration Tab</td></tr>
<tr><td>RS232 Port</td><td>DUT MediaLB Interface Mode</td><td>DUT MediaLB Clock Speed</td><td>DUT MOST Target Address</td><td></td><td></td><td></td><td></td></tr>
<tr><td>User configurable</td><td>6-Pin</td><td>3072xFs</td><td>0101h</td><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="8">Asynchronous Data Test Tab</td></tr>
<tr><td>Tx Channel Address</td><td>Rx Channel Address</td><td>Blockwidth (quadlets/ frame)</td><td>MEP</td><td>MEP Destination Address</td><td>MEP Source Address</td><td></td><td></td></tr>
<tr><td>0x0006</td><td>0x0008</td><td>27</td><td>Disable</td><td>-</td><td>-</td><td></td><td></td></tr>
<tr><td>Varied Packet Length</td><td>Fixed Length (bytes)</td><td>Minimum Length (bytes)</td><td>Maximum Length (bytes)</td><td>Increments (bytes)</td><td>Repetitions (pkts)</td><td></td><td></td></tr>
<tr><td>Enable</td><td>-</td><td>6</td><td>1014</td><td>1</td><td>1</td><td></td><td></td></tr>
<tr><td>Continuous Test</td><td>Test Duration (pkts)</td><td>Packet Delay (µs)</td><td>Packet Counter</td><td>Pattern Type</td><td></td><td></td><td></td></tr>
<tr><td>Disable</td><td>5000</td><td>6000</td><td>Enable</td><td>Random</td><td></td><td></td><td></td></tr>
</table>

Table 8-51: mitb_t2651_6pin_3072fs_a_27q

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8.3.24 mitb_t2660_6pin_4096fs_a_1q

Test Name	*mitb_t2660_6pin_4096fs_a_1q*						
Test Characteristic	Basic 4096xFs test - Concurrent Rx and Tx transfer of MediaLB asynchronous data - Blockwidth 2 x 1 quadlet per frame - Fixed Packet Length 32 Bytes - Packet Delay 2000 us						
Test Configuration Files	*mitb_t2660_6pin_4096fs_a_1q_cfg_setup.txt* *mitb_t2660_6pin_4096fs_a_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	4096xFs	Async	PC0	0x01FE		
				PC1	0x0006	Async Rx	
				PC2	0x0008	Async Tx	
				…	…	…	
				PC116	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	4096xFs	0101h				
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	32	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Enable	5000	2000	Enable	Byte Counter			

Table 8-52: mitb_t2660_6pin_2048fs_a_1q

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8.4 Synchronous Tests

The following table provides an overview of available synchronous data tests.

Overview Synchronous Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t3310_3pin_256fs_s_1q	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t3320_3pin_512fs_s_1q	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t3330_3pin_1024fs_s_1q	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t3331_3pin_1024fs_s_3q	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 3 quadlet per frame - CA=0x003C & CA=0x003E
mitb_t3332_3pin_1024fs_s_3q	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 3 quadlet per frame - CA=0x003C & CA=0x003E
mitb_t3333_3pin_1024fs_s_7q	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 7 quadlet per frame
mitb_t3334_3pin_1024fs_s_7q	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 7 quadlet per frame
mitb_t3335_3pin_1024fs_s_15q	1024xFs test with high blockwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame
MediaLB 6-pin Tests	
mitb_t3640_6pin_2048fs_s_1q	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t3641_6pin_2048fs_s_15q	2048xFs test with 2 x 15 quadlets blockwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame
mitb_t3642_6pin_2048fs_s_4q	2048xFs test with ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 4 quadlet per frame - CA=0x0042 & CA=0x007E

Table 8-53: Synchronous Test Overview (Part 1)

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Overview Synchronous Tests	
Test Name	**Test Characteristics**
MediaLB 6-pin Tests	
mitb_t3650_6pin_3072fs_s_1q	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t3651_6pin_3072fs_s_15q	3072xFs test with maximum bandwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame
mitb_t3660_6pin_4096fs_s_1q	Basic 4096xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t3661_6pin_4096fs_s_15q	4096xFs test with maximum bandwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame

Table 8-54: Synchronous Test Overview (Part 2)

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8.4.1 mitb_t3310_3pin_256fs_s_1q

Test Name	***mitb_t3310_3pin_256fs_s_1q***						
Description	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t3310_3pin_256fs_s_1q_cfg_setup.txt* *mitb_t3310_3pin_256fs_s_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	256xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				PC2	0x000C	Sync Tx	
				…	…		
				PC7	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	256xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-55: mitb_t3310_3pin_256fs_s_1q

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8.4.2 mitb_t3320_3pin_512fs_s_1q

Test Name	*mitb_t3320_3pin_512fs_s_1q*						
Description	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t3320_3pin_512fs_s_1q_cfg_setup.txt* *mitb_t3320_3pin_512fs_s_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	512xFs	Sync	PC0	0x01FE		
				PC1	0x0012	Sync Rx	
				PC2	0x0014	Sync Tx	
				…	…		
				PC15	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	512xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x0012	0x0014	1	Enable	Byte Counter			

Table 8-56: mitb_t3320_3pin_512fs_s_1q

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8.4.3 mitb_t3330_3pin_1024fs_s_1q

Test Name	***mitb_t3330_3pin_1024fs_s_1q***						
Description	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t3330_3pin_1024fs_s_1q_cfg_setup.txt* *mitb_t3330_3pin_1024fs_s_1q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Sync	PC0	0x01FE		
				PC1	0x0016	Sync Rx	
				PC2	0x0018	Sync Tx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x0016	0x0018	1	Enable	Byte Counter			

Table 8-57: mitb_t3330_3pin_1024fs_s_1q

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8.4.4 mitb_t3331_3pin_1024fs_s_3q

Test Name	*mitb_t3331_3pin_1024fs_s_3q*						
Description	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 3 quadlet per frame - CA=0x003C & CA=0x003E						
Test Configuration Files	*mitb_t3331_3pin_1024fs_s_3q_cfg_setup.txt* *mitb_t3331_3pin_1024fs_s_3q_cfg_start.txt*			Manual setup of test via GUI possible?	No		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Sync	PC0	0x01FE		
				PC1	0x003C	Sync Rx	
				PC2	0x003E	Sync Tx	
				PC3	0x003C	Sync Rx	
				PC4	0x003C	Sync Rx	
				PC5	0x003E	Sync Tx	
				PC6	0x003E	Sync Tx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x003C	0x003E	3	Enable	Byte Counter			

Table 8-58: mitb_t3331_3pin_1024fs_s_3q

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8.4.5 mitb_t3332_3pin_1024fs_s_3q

Test Name	*mitb_t3332_3pin_1024fs_s_3q*						
Description	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 3 quadlet per frame - CA=0x003C & CA=0x003E						
Test Configuration Files	*mitb_t3332_3pin_1024fs_s_3q_cfg_setup.txt* *mitb_t3332_3pin_1024fs_s_3q_cfg_start.txt*			Manual setup of test via GUI possible?	No		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Sync	PC0	0x01FE		
				PC1	0x003E	Sync Tx	
				PC2	0x003C	Sync Rx	
				PC3	0x003E	Sync Tx	
				PC4	0x003E	Sync Tx	
				PC5	0x003C	Sync Rx	
				PC6	0x003C	Sync Rx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x003C	0x003E	3	Enable	Byte Counter			

Table 8-59: mitb_t3332_3pin_1024fs_s_3q

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8.4.6 mitb_t3333_3pin_1024fs_s_7q

Test Name	*mitb_t3333_3pin_1024fs_s_7q*						
Description	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 7 quadlet per frame						
Test Configuration Files	*mitb_t3333_3pin_1024fs_s_7q_cfg_setup.txt* *mitb_t3333_3pin_1024fs_s_7q_cfg_start.txt*				Manual setup of test via GUI possible?	No	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				PC2	0x000C	Sync Tx	
				PC3	0x000A	Sync Rx	
				PC4	0x000A	Sync Rx	
				PC5	0x000C	Sync Tx	
				PC6	0x000C	Sync Tx	
				PC7	0x000A	Sync Rx	
				PC8	0x000A	Sync Rx	
				PC9	0x000A	Sync Rx	
				PC10	0x000C	Sync Tx	
				PC11	0x000C	Sync Tx	
				PC12	0x000C	Sync Tx	
				PC13	0x000A	Sync Rx	
				PC14	0x000C	Sync Tx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	7	Enable	Byte Counter			

Table 8-60: mitb_t3333_3pin_1024fs_s_7q

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8.4.7 mitb_t3334_3pin_1024fs_s_7q

Test Name	*mitb_t3334_3pin_1024fs_s_7q*						
Description	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 7 quadlet per frame						
Test Configuration Files	*mitb_t3334_3pin_1024fs_s_7q_cfg_setup.txt* *mitb_t3334_3pin_1024fs_s_7q_cfg_start.txt*				Manual setup of test via GUI possible?	No	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Sync	PC0	0x01FE		
				PC1	0x000C	Sync Tx	
				PC2	0x000A	Sync Rx	
				PC3	0x000C	Sync Tx	
				PC4	0x000C	Sync Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000A	Sync Rx	
				PC7	0x000C	Sync Tx	
				PC8	0x000C	Sync Tx	
				PC9	0x000C	Sync Tx	
				PC10	0x000A	Sync Rx	
				PC11	0x000A	Sync Rx	
				PC12	0x000A	Sync Rx	
				PC13	0x000C	Sync Tx	
				PC14	0x000A	Sync Rx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	7	Enable	Byte Counter			

Table 8-61: mitb_t3334_3pin_1024fs_s_7q

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8.4.8 mitb_t3335_3pin_1024fs_s_15q

Test Name	*mitb_t3335_3pin_1024fs_s_15q*						
Description	1024xFs test with high blockwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame						
Test Configuration Files	*mitb_t3335_3pin_1024fs_s_15q_cfg_setup.txt* *mitb_t3335_3pin_1024fs_s_15q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				…	…	…	
				PC15	0x000A	Sync Rx	
				PC16	0x000C	Sync Tx	
				…	…	…	
				PC30	0x000C	Sync Tx	
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	15	Enable	Byte Counter			

Table 8-62: mitb_t3335_3pin_1024fs_s_15q

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8.4.9 mitb_t3640_6pin_2048fs_s_1q

Test Name	***mitb_t3640_6pin_2048fs_s_1q***						
Description	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t3640_6pin_2048fs_s_1q_cfg_setup.txt* *mitb_t3640_6pin_2048fs_s_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				PC2	0x000C	Sync Tx	
				…	…		
				PC57	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-63: mitb_t3640_6pin_2048fs_s_1q

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8.4.10 mitb_t3641_6pin_2048fs_s_15q

Test Name	*mitb_t3641_6pin_2048fs_s_15q*						
Description	2048xFs test with 2 x 15 quadlets blockwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame						
Test Configuration Files	*mitb_t3641_6pin_2048fs_s_15q_cfg_setup.txt* *mitb_t3641_6pin_2048fs_s_15q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				…	…	…	
				PC15	0x000A	Sync Rx	
				PC16	0x000C	Sync Tx	
				…	…	…	
				PC30	0x000C	Sync Tx	
				…	…		
				PC57	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	15	Enable	Byte Counter			

Table 8-64: mitb_t3641_6pin_2048fs_s_15q

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8.4.11 mitb_t3642_6pin_2048fs_s_4q

Test Name	*mitb_t3642_6pin_2048fs_s_4q*						
Description	2048xFs test with ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 4 quadlet per frame - CA=0x0042 & CA=0x007E						
Test Configuration Files	*mitb_t3642_6pin_2048fs_s_4q_cfg_setup.txt* *mitb_t3642_6pin_2048fs_s_4q_cfg_start.txt*				Manual setup of test via GUI possible?		YES
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Sync	PC0	0x01FE		
				PC1	0x0042	Sync Rx	
				…	…	…	
				PC4	0x0042	Sync Rx	
				PC5	0x007E	Sync Tx	
				…	…	…	
				PC8	0x007E	Sync Tx	
				…	…		
				PC57	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x0042	0x007E	4	Enable	Byte Counter			

Table 8-65: mitb_t3642_6pin_2048fs_s_4q

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8.4.12 mitb_t3650_6pin_3072fs_s_1q

Test Name	***mitb_t3650_6pin_3072fs_s_1q***						
Description	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t3650_6pin_3072fs_s_1q_cfg_setup.txt* *mitb_t3650_6pin_3072fs_s_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	3072xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				PC2	0x000C	Sync Tx	
				…	…		
				PC86	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	3072xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-66: mitb_t3650_6pin_3072fs_s_1q

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8.4.13 mitb_t3651_6pin_3072fs_s_15q

Test Name	***mitb_t3651_6pin_3072fs_s_15q***						
Description	3072xFs test with maximum bandwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame						
Test Configuration Files	*mitb_t3651_6pin_3072fs_s_15q_cfg_setup.txt* *mitb_t3651_6pin_3072fs_s_15q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	3072xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				…	…	…	
				PC15	0x000A	Sync Rx	
				PC16	0x000C	Sync Tx	
				…	…	…	
				PC30	0x000C	Sync Tx	
				…	…		
				PC86	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	3072xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	15	Enable	Byte Counter			

Table 8-67: mitb_t3651_6pin_3072fs_s_15q

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8.4.14 mitb_t3660_6pin_4096fs_s_1q

Test Name	***mitb_t3660_6pin_4096fs_s_1q***						
Description	Basic 4096xFs test - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t3660_6pin_4096fs_s_1q_cfg_setup.txt* *mitb_t3660_6pin_4096fs_s_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	4096xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				PC2	0x000C	Sync Tx	
				…	…		
				PC116	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	4096xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-68: mitb_t3660_6pin_4096fs_s_1q

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8.4.15 mitb_t3661_6pin_4096fs_s_15q

Test Name	***mitb_t3661_6pin_4096fs_s_15q***						
Description	4096xFs test with maximum bandwidth - Concurrent Rx and Tx transfer of MediaLB synchronous data - Blockwidth 2 x 15 quadlet per frame						
Test Configuration Files	*mitb_t3661_6pin_4096fs_s_15q_cfg_setup.txt* *mitb_t3661_6pin_4096fs_s_15q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	4096xFs	Sync	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				…	…	…	
				PC15	0x000A	Sync Rx	
				PC16	0x000C	Sync Tx	
				…	…	…	
				PC30	0x000C	Sync Tx	
				…	…		
				PC116	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	4096xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	15	Enable	Byte Counter			

Table 8-69: mitb_t3661_6pin_4096fs_s_15q

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8.5 Isochronous Tests

The following table provides an overview of available isochronous data tests.

Overview Isochronous Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t4310_3pin_256fs_i_1q	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t4320_3pin_512fs_i_1q	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t4330_3pin_1024fs_i_1q	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t4331_3pin_1024fs_i_7q	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 7 quadlet per frame - CA=0x003C & CA=0x003E
mitb_t4332_3pin_1024fs_i_7q	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 7 quadlet per frame - CA=0x003C & CA=0x003E
mitb_t4333_3pin_1024fs_i_15q	1024xFs test with maximum blockwidth - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 15 quadlet per frame
mitb_t4334_3pin_1024fs_i_15q	1024xFs test with Packet Size 196 Bytes - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 15 quadlet per frame
mitb_t4337_3pin_1024fs_i_15q	1024xFs test with Flow Control enabled, packet size 188 bytes - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth: Tx channel 15 quadlet per frame, Rx channel 1 quadlet per frame

Table 8-70: Isochronous Test Overview (Part 1)

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Overview Isochronous Tests	
Test Name	**Test Characteristics**
MediaLB 6-pin Tests	
mitb_t4640_6pin_2048fs_i_1q	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t4641_6pin_2048fs_i_27q	2048xFs test with maximum blockwidth - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 27 quadlet per frame
mitb_t4642_6pin_2048fs_i_4q	2048xFs test with ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 4 quadlet per frame - CA=0x007E & CA=0x7C
mitb_t4650_6pin_3072fs_i_1q	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame
mitb_t4651_6pin_3072fs_i_27q	3072xFs test with maximum blockwidth - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 27 quadlet per frame - Packet size 196 bytes

Table 8-71: Isochronous Test Overview (Part 2)

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8.5.1 mitb_t4310_3pin_256fs_i_1q

Test Name	***mitb_t4310_3pin_256fs_i_1q***						
Description	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t4310_3pin_256fs_i_1q_cfg_setup.txt* *mitb_t4310_3pin_256fs_i_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	256xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				PC2	0x0010	Isoc Tx	
				…	…		
				PC7	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	256xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-72: mitb_t4310_3pin_256fs_i_1q

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8.5.2 mitb_t4320_3pin_512fs_i_1q

Test Name	***mitb_t4320_3pin_512fs_i_1q***						
Description	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t4320_3pin_512fs_i_1q_cfg_setup.txt* *mitb_t4320_3pin_512fs_i_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	512xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				PC2	0x0010	Isoc Tx	
				…	…		
				PC15	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	512xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-73: mitb_t4320_3pin_512fs_i_1q

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8.5.3 mitb_t4330_3pin_1024fs_i_1q

Test Name	*mitb_t4330_3pin_1024fs_i_1q*						
Description	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t4330_3pin_1024fs_i_1q_cfg_setup.txt* *mitb_t4330_3pin_1024fs_i_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				PC2	0x0010	Isoc Tx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-74: mitb_t4330_3pin_1024fs_i_1q

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8.5.4 mitb_t4331_3pin_1024fs_i_7q

Test Name	*mitb_t4331_3pin_1024fs_i_7q*						
Description	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 7 quadlet per frame - CA=0x003C & CA=0x003E						
Test Configuration Files	*mitb_t4331_3pin_1024fs_i_7q_cfg_setup.txt* *mitb_t4331_3pin_1024fs_i_7q_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Isoc	PC0	0x01FE		
				PC1	0x003C	Isoc Rx	
				PC2	0x003E	Isoc Tx	
				PC3	0x003C	Isoc Rx	
				PC4	0x003C	Isoc Rx	
				PC5	0x003E	Isoc Tx	
				PC6	0x003E	Isoc Tx	
				PC7	0x003C	Isoc Rx	
				PC8	0x003C	Isoc Rx	
				PC9	0x003C	Isoc Rx	
				PC10	0x003E	Isoc Tx	
				PC11	0x003E	Isoc Tx	
				PC12	0x003E	Isoc Tx	
				PC13	0x003C	Isoc Rx	
				PC14	0x003E	Isoc Tx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x003C	0x003E	7	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-75: mitb_t4331_3pin_1024fs_i_7q

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8.5.5 mitb_t4332_3pin_1024fs_i_7q

Test Name	*mitb_t4332_3pin_1024fs_i_7q*						
Description	1024xFs test with alternating Tx/Rx ChannelAddresses - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 7 quadlet per frame - CA=0x003C & CA=0x003E						
Test Configuration Files	*mitb_t4332_3pin_1024fs_i_7q_cfg_setup.txt* *mitb_t4332_3pin_1024fs_i_7q_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Isoc	PC0	0x01FE		
				PC1	0x003E	Isoc Tx	
				PC2	0x003C	Isoc Rx	
				PC3	0x003E	Isoc Tx	
				PC4	0x003E	Isoc Tx	
				PC5	0x003C	Isoc Rx	
				PC6	0x003C	Isoc Rx	
				PC7	0x003E	Isoc Tx	
				PC8	0x003E	Isoc Tx	
				PC9	0x003E	Isoc Tx	
				PC10	0x003C	Isoc Rx	
				PC11	0x003C	Isoc Rx	
				PC12	0x003C	Isoc Rx	
				PC13	0x003E	Isoc Tx	
				PC14	0x003C	Isoc Rx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x003C	0x003E	7	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-76: mitb_t4332_3pin_1024fs_i_7q

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8.5.6 mitb_t4333_3pin_1024fs_i_15q

Test Name	*mitb_t4333_3pin_1024fs_i_15q*						
Description	1024xFs test with maximum blockwidth - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 15 quadlet per frame						
Test Configuration Files	*mitb_t4333_3pin_1024fs_i_15q_cfg_setup.txt* *mitb_t4333_3pin_1024fs_i_15q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				…	…	…	
				PC15	0x000E	Isoc Rx	
				PC16	0x0010	Isoc Tx	
				…	…	…	
				PC30	0x0010	Isoc Tx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	15	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-77: mitb_t4333_3pin_1024fs_i_15q

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8.5.7 mitb_t4334_3pin_1024fs_i_15q

Test Name	*mitb_t4334_3pin_1024fs_i_15q*						
Description	1024xFs test with Packet Size 196 Bytes - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 15 quadlet per frame						
Test Configuration Files	*mitb_t4334_3pin_1024fs_i_15q_cfg_setup.txt* *mitb_t4334_3pin_1024fs_i_15q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				…	…	…	
				PC15	0x000E	Isoc Rx	
				PC16	0x0010	Isoc Tx	
				…	…	…	
				PC30	0x0010	Isoc Tx	
				…	…		
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	15	Disable	196	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-78: mitb_t4334_3pin_1024fs_i_15q

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8.5.8 mitb_t4337_3pin_1024fs_i_15q

Test Name	*mitb_t4337_3pin_1024fs_i_15q*						
Description	1024xFs test with Flow Control enabled, packet size 188 bytes - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth Tx channel 15 quadlet per frame - Blockwidth Rx channel 1 quadlet per frame ***Note*** Test fails with missed packets due to INIC overflow on Rx channel to force RxBusy responses on both channels; missed packets due discarded isoc data on MOST because of INIC overflow.						
Test Configuration Files	*mitb_t4337_3pin_1024fs_i_15q_cfg_setup.txt* *mitb_t4337_3pin_1024fs_i_15q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				…	…	…	
				PC15	0x000E	Isoc Rx	
				PC16	0x0010	Isoc Tx	
				…	…	…	
				PC31	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth Tx *(quadlets/ frame)*	Blockwidth Rx *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*	
0x000E	0x0010	15	1	Disable	188	3000	
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	10.000	Enable	Byte Counter				

Table 8-79: mitb_t4337_3pin_1024fs_i_15q

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8.5.9 mitb_t4640_6pin_2048fs_i_1q

Test Name	*mitb_t4640_6pin_2048fs_i_1q*						
Description	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t4640_6pin_2048fs_i_1q_cfg_setup.txt* *mitb_t4640_6pin_2048fs_i_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				PC2	0x0010	Isoc Tx	
				…	…		
				PC57	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-80: mitb_t4640_6pin_2048fs_i_1q

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8.5.10 mitb_t4641_6pin_2048fs_i_27q

Test Name	*mitb_t4641_6pin_2048fs_i_27q*						
Description	2048xFs test with maximum blockwidth - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 27 quadlet per frame						
Test Configuration Files	*mitb_t4641_6pin_2048fs_i_27q_cfg_setup.txt* *mitb_t4641_6pin_2048fs_i_27q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				…	…	…	
				PC27	0x000E	Isoc Rx	
				PC28	0x0010	Isoc Tx	
				…	…	…	
				PC54	0x0010	Isoc Tx	
				…	…		
				PC57	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	27	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-81: mitb_t4641_6pin_2048fs_i_27q

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8.5.11 mitb_t4642_6pin_2048fs_i_4q

Test Name	*mitb_t4642_6pin_2048fs_i_4q*						
Description	2048xFs test with ChannelAddresses in the upper address range - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 4 quadlet per frame - CA=0x007E & CA=0x7C						
Test Configuration Files	*mitb_t4642_6pin_2048fs_i_4q_cfg_setup.txt* *mitb_t4642_6pin_2048fs_i_4q_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Isoc	PC0	0x01FE		
				PC1	0x007E	Isoc Rx	
				…	…	…	
				PC4	0x007E	Isoc Rx	
				PC5	0x007C	Isoc Tx	
				…	…	…	
				PC10	0x007C	Isoc Tx	
				…	…		
				PC57	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x007E	0x007C	4	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	1000	Enable	Byte Counter				

Table 8-82: mitb_t4642_6pin_2048fs_i_4q

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8.5.12 mitb_t4650_6pin_3072fs_i_1q

Test Name	*mitb_t4650_6pin_3072fs_i_1q*						
Description	Basic 3072xFs test - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 1 quadlet per frame						
Test Configuration Files	*mitb_t4650_6pin_3072fs_i_1q_cfg_setup.txt* *mitb_t4650_6pin_3072fs_i_1q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	3072xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				PC2	0x0010	Isoc Tx	
				…	…		
				PC86	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	3072xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-83: mitb_t4650_6pin_3072fs_i_1q

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8.5.13 mitb_t4651_6pin_3072fs_i_27q

Test Name	*mitb_t4651_6pin_3072fs_i_27q*						
Description	3072xFs test with maximum blockwidth - Concurrent Rx and Tx transfer of MediaLB isochronous data - Blockwidth 2 x 27 quadlet per frame - Packet size 196 bytes						
Test Configuration Files	*mitb_t4651_6pin_3072fs_i_27q_cfg_setup.txt* *mitb_t4651_6pin_3072fs_i_27q_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	3072xFs	Isoc	PC0	0x01FE		
				PC1	0x000E	Isoc Rx	
				…	…	…	
				PC27	0x000E	Isoc Rx	
				PC28	0x0010	Isoc Tx	
				…	…	…	
				PC54	0x0010	Isoc Tx	
				…	…		
				PC86	0x0000		
PGA GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Pin Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	3072xFs	0101h				
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	27	Disable	196	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-84: mitb_t4651_6pin_3072fs_i_27q

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8.6 Combined Tests

The following table provides an overview of available combined data tests.

Overview Combined Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t5310_3pin_256fs_cas	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per data type - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s
mitb_t5320_3pin_512fs_cas	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s
mitb_t5330_3pin_1024fs_cas	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s
mitb_t5331_3pin_1024fs_casi	1024xFs test, 4 data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed packet/msg length: control 8 bytes, asynchronous 14 bytes, isochronous 188 bytes - Packet Delay 12.000 us, Message Throughput 50mgs/s, 1000 kbit/s
mitb_t5332_3pin_1024fs_casi	1024xFs test, all data types, varied transfer parameter - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Varied msg/packet length control/async, packet size Isochronous 196 bytes - Packet delay 12.000 us, message throughput 50mgs/s, packet throughput 1000 kbit/s
mitb_t5333_3pin_1024fs_csi	1024xFs test, 3 data types - Concurrent Rx and Tx transfer of MediaLB control, synchronous and isochronous data - Blockwidth 2 x 4 quadlet per frame per loopback - Control Fixed Packet Length 8 bytes, 188 bytes Isoc Blocksize - Message Throughput 50mgs/s, 1000 kbit/s

Table 8-85: Combined Test Overview (Part 1)

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Overview Combined Tests	
Test Name	**Test Characteristics**
MediaLB 6-pin Tests	
mitb_t5640_6pin_2048fs_cas	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length: Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s
mitb_t5641_6pin_2048fs_si	2048xFs test, 2 streaming loopbacks - Concurrent Rx and Tx transfer of MediaLB synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - packet size 188 bytes, packet throughput 1000 kbit/s
mitb_t5642_6pin_2048fs_casi	2048xFs test, all data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed packet/msg length: control 8 bytes, asynchronous 14 bytes, isochronous 188 bytes - Packet Delay 12.000 us, message Throughput 50mgs/s, packet throughput 1000 kbit/s
mitb_t5643_6pin_2048fs_casi	2048xFs test, all data types, varied transfer parameter - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Varied msg/packet length control/async, packet size Isochronous 196 bytes - Packet delay 12.000 us, message throughput 50mgs/s, packet throughput 1000 kbit/s

Table 8-86: Combined Test Overview (Part 2)

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8.6.1 mitb_t5310_3pin_256fs_cas

Test Name	*mitb_t5310_3pin_256fs_cas*						
Test Characteristic	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per data type - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5310_3pin_256fs_cas_cfg_setup.txt* *mitb_t5310_3pin_256fs_cas_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	256xFs	Control, Async, Sync	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				PC7	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	256xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	10000	450	Enable	Byte Counter			

Table 8-87: mitb_t5310_3pin_256fs_cas (Part 1)

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Test Name	*mitb_t5310_3pin_256fs_cas*						
Test Characteristic	Basic 256xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per data type - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5310_3pin_256fs_cas_cfg_setup.txt* *mitb_t5310_3pin_256fs_cas_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	10000	2000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-88: mitb_t5310_3pin_256fs_cas (Part 2)

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8.6.2 mitb_t5320_3pin_512fs_cas

Test Name	*mitb_t5320_3pin_512fs_cas*						
Test Characteristic	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5320_3pin_512fs_cas_cfg_setup.txt* *mitb_t5320_3pin_512fs_cas_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	512xFs	Control, Async, Sync	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				…	…		
				PC15	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	512xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	10000	450	Enable	Byte Counter			

Table 8-89: mitb_t5320_3pin_512fs_cas (Part 1)

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Test Name	*mitb_t5320_3pin_512fs_cas*						
Test Characteristic	Basic 512xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5320_3pin_512fs_cas_cfg_setup.txt* *mitb_t5320_3pin_512fs_cas_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	10000	2000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-90: mitb_t5320_3pin_512fs_cas (Part 2)

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8.6.3 mitb_t5330_3pin_1024fs_cas

Test Name	*mitb_t5330_3pin_1024fs_cas*						
Test Characteristic	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5330_3pin_1024fs_cas_cfg_setup.txt* *mitb_t5330_3pin_1024fs_cas_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control, Async, Sync	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	10000	450	Enable	Byte Counter			

Table 8-91: mitb_t5330_3pin_1024fs_cas (Part 1)

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Test Name	*mitb_t5330_3pin_1024fs_cas*						
Test Characteristic	Basic 1024xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5330_3pin_1024fs_cas_cfg_setup.txt* *mitb_t5330_3pin_1024fs_cas_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	10000	2000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-92: mitb_t5330_3pin_1024fs_cas (Part 2)

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8.6.4 mitb_t5331_3pin_1024fs_casi

Test Name	*mitb_t5331_3pin_1024fs_casi*						
Test Characteristic	1024xFs test, 4 data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed packet/msg length: control 8 bytes, asynchronous 14 bytes, isochronous 188 bytes - Packet Delay 12.000 us, Message Throughput 50mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5331_3pin_1024fs_casi_cfg_setup.txt* *mitb_t5331_3pin_1024fs_casi_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control, Async, Sync, Isoc	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				PC7	0x000E	Isoc Rx	
				PC8	0x0010	Isoc Tx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				Trigger on Error
User configurable	3-Pin	1024xFs	0101h				Disable
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	50	Enable	Byte Counter			

Table 8-93: mitb_t5331_3pin_1024fs_casi (Part 1)

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Test Name	*mitb_t5331_3pin_1024fs_casi*						
Test Characteristic	1024xFs test, 4 data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed packet/msg length: control 8 bytes, asynchronous 14 bytes, isochronous 188 bytes - Packet Delay 12.000 us, Message Throughput 50mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5331_3pin_1024fs_casi_cfg_setup.txt* *mitb_t5331_3pin_1024fs_casi_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	12.000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-94: mitb_t5331_3pin_1024fs_casi (Part 2)

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8.6.5 mitb_t5332_3pin_1024fs_casi

Test Name	*mitb_t5332_3pin_1024fs_casi*						
Test Characteristic	1024xFs test, 4 data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed packet/msg length: control 8 bytes, asynchronous 14 bytes, isochronous 188 bytes - Packet Delay 12.000 us, Message Throughput 50mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5332_3pin_1024fs_casi_cfg_setup.txt* *mitb_t5332_3pin_1024fs_casi_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control, Async, Sync, Isoc	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				PC7	0x000E	Isoc Rx	
				PC8	0x0010	Isoc Tx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				Trigger on Error
User configurable	3-Pin	1024xFs	0101h				Disable
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Enable	-	6	45	1	1		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	50	Enable	Byte Counter			

Table 8-95: mitb_t5332_3pin_1024fs_casi (Part 1)

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Test Name	*mitb_t5332_3pin_1024fs_casi*						
Test Characteristic	1024xFs test, 4 data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed packet/msg length: control 8 bytes, asynchronous 14 bytes, isochronous 188 bytes - Packet Delay 12.000 us, Message Throughput 50mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5332_3pin_1024fs_casi_cfg_setup.txt* *mitb_t5332_3pin_1024fs_casi_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	6	1014	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	12.000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	196	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	10.000	Enable	Byte Counter				

Table 8-96: mitb_t5332_3pin_1024fs_casi (Part 2)

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8.6.6 mitb_t5333_3pin_1024fs_csi

Test Name	*mitb_t5333_3pin_1024fs_csi*						
Test Characteristic	1024xFs test, 3 data types - Concurrent Rx and Tx transfer of MediaLB control, synchronous and isochronous data - Blockwidth 2 x 4 quadlet per frame per loopback - Control Fixed Packet Length 8 bytes, 188 bytes Isoc Blocksize - Message Throughput 50mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5333_3pin_1024fs_csi_cfg_setup.txt* *mitb_t5333_3pin_1024fs_csi_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	Control, Sync, Isoc	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				PC7	0x000E	Isoc Rx	
				PC8	0x0010	Isoc Tx	
				…	…		
				PC31	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				Trigger on Error
User configurable	3-Pin	1024xFs	0101h				Disable
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	50	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-97: mitb_t5333_3pin_1024fs_csi (Part 1)

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Test Name	*mitb_t5333_3pin_1024fs_csi*						
Test Characteristic	1024xFs test, 3 data types - Concurrent Rx and Tx transfer of MediaLB control, synchronous and isochronous data - Blockwidth 2 x 4 quadlet per frame per loopback - Control Fixed Packet Length 8 bytes, 188 bytes Isoc Blocksize - Message Throughput 50mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5333_3pin_1024fs_csi_cfg_setup.txt* *mitb_t5333_3pin_1024fs_csi_cfg_start.txt*				Manual setup of test via GUI possible?		NO
GUI Configuration							
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	20.000	Enable	Byte Counter				

Table 8-98: mitb_t5333_3pin_1024fs_csi (Part 2)

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8.6.7 mitb_t5640_6pin_2048fs_cas

Test Name	*mitb_t5640_6pin_2048fs_cas*						
Test Characteristic	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length: Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5640_6pin_2048fs_cas_cfg_setup.txt* *mitb_t5640_6pin_2048fs_cas_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control, Async, Sync	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				…			
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	10000	450	Enable	Byte Counter			

Table 8-99: mitb_t5640_6pin_2048fs_cas (Part 1)

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Test Name	*mitb_t5640_6pin_2048fs_cas*						
Test Characteristic	Basic 2048xFs test - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length: Control 8 bytes, Asynchronous 14 bytes - Packet Delay 2000 us, message Throughput 450mgs/s						
Test Configuration Files	*mitb_t5640_6pin_2048fs_cas_cfg_setup.txt* *mitb_t5640_6pin_2048fs_cas_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	10000	2000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			

Table 8-100: mitb_t5640_6pin_2048fs_cas (Part 2)

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8.6.8 mitb_t5641_6pin_2048fs_si

Test Name	*mitb_t5641_6pin_2048fs_si*						
Test Characteristic	2048xFs test, 2 streaming loopbacks - Concurrent Rx and Tx transfer of MediaLB synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - packet size 188 bytes, packet throughput 1000 kbit/s						
Test Configuration Files	*mitb_t5641_6pin_2048fs_si_cfg_setup.txt* *mitb_t5641_6pin_2048fs_si_cfg_start.txt*				Manual setup of test via GUI possible?	NO	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Sync, Isoc	PC0	0x01FE		
				PC1	0x000A	Sync Rx	
				PC2	0x000C	Sync Tx	
				PC3	0x000E	Isoc Rx	
				PC4	0x0010	Isocc Tx	
				…			
				PC57	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	10.000	Enable	Byte Counter				

Table 8-101: mitb_t5641_6pin_2048fs_si

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8.6.9 mitb_t5642_6pin_2048fs_casi

Test Name	*mitb_t5462_6pin_2048fs_casi*						
Test Characteristic	1024xFs test, 4 data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes, 188 bytes Isoc Blocksize - Packet Delay 2000 us, message Throughput 450mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5462_6pin_2048fs_casi_cfg_setup.txt* *mitb_t5462_6pin_2048fs_casi_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control, Async, Sync, Isoc	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				PC7	0x000E	Isoc Rx	
				PC8	0x0010	Isoc Tx	
				…	…		
				PC57	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				Trigger on Error
User configurable	6-Pin	2048xFs	0101h				Disable
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Disable	8	-	-	-	-		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	50	Enable	Byte Counter			

Table 8-102: mitb_t5642_6pin_2048fs_casi (Part 1)

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Test Name	*mitb_t5462_6pin_2048fs_casi*						
Test Characteristic	1024xFs test, 4 data types - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Fixed Packet Length, Control 8 bytes, Asynchronous 14 bytes, 188 bytes Isoc Blocksize - Packet Delay 2000 us, message Throughput 450mgs/s, 1000 kbit/s						
Test Configuration Files	*mitb_t5462_6pin_2048fs_casi_cfg_setup.txt* *mitb_t5462_6pin_2048fs_casi_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Disable	14	-	-	-	-		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	12.000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	188	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	5000	Enable	Byte Counter				

Table 8-103: mitb_t5642_6pin_2048fs_casi (Part 2)

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8.6.10 mitb_t5643_6pin_2048fs_casi

Test Name	*mitb_t5463_6pin_2048fs_casi*						
Test Characteristic	2048xFs test, all data types, varied transfer parameter - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Varied msg/packet length control/async, packet size Isochronous 196 bytes - Packet delay 12.000 us, message throughput 50mgs/s, packet throughput 1000 kbit/s						
Test Configuration Files	*mitb_t5463_6pin_2048fs_casi_cfg_setup.txt* *mitb_t5463_6pin_2048fs_casi_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Types	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	Control, Async, Sync, Isoc	PC0	0x01FE		
				PC1	0x0004	Control Tx	
				PC2	0x0002	Control Rx	
				PC3	0x0006	Async Rx	
				PC4	0x0008	Async Tx	
				PC5	0x000A	Sync Rx	
				PC6	0x000C	Sync Tx	
				PC7	0x000E	Isoc Rx	
				PC8	0x0010	Isoc Tx	
				…	…		
				PC57	0x003E		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				Trigger on Error
User configurable	6-Pin	2048xFs	0101h				Disable
Control Data Test Tab							
Tx Channel Address	Rx Channel Address						
0x0002	0x0004						
Varied Message Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(msgs)*		
Enable	-	6	45	1	1		
Continuous Test	Test Duration *(msgs)*	Throughput *(msgs/s)*	Message Counter	Pattern Type			
Disable	5000	50	Enable	Byte Counter			

Table 8-104: mitb_t5643_6pin_2048fs_casi (Part 1)

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Test Name	*mitb_t5463_6pin_2048fs_casi*						
Test Characteristic	2048xFs test, all data types, varied transfer parameter - Concurrent Rx and Tx transfer of MediaLB control, asynchronous, synchronous and isochronous data - Blockwidth 2 x 1 quadlet per frame per loopback - Varied msg/packet length control/async, packet size Isochronous 196 bytes - Packet delay 12.000 us, message throughput 50mgs/s, packet throughput 1000 kbit/s						
Test Configuration Files	*mitb_t5463_6pin_2048fs_casi_cfg_setup.txt* *mitb_t5463_6pin_2048fs_casi_cfg_start.txt*			Manual setup of test via GUI possible?	NO		
GUI Configuration							
Asynchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	MEP	MEP Destination Address	MEP Source Address		
0x0006	0x0008	1	Disable	-	-		
Varied Packet Length	Fixed Length *(bytes)*	Minimum Length *(bytes)*	Maximum Length *(bytes)*	Increments *(bytes)*	Repetitions *(pkts)*		
Enable	-	22	502	1	1		
Continuous Test	Test Duration *(pkts)*	Packet Delay *(µs)*	Packet Counter	Pattern Type			
Disable	5000	12.000	Enable	Byte Counter			
Synchronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Frame Counter	Pattern Type			
0x000A	0x000C	1	Enable	Byte Counter			
Isochronous Data Test Tab							
Tx Channel Address	Rx Channel Address	Blockwidth *(quadlets/ frame)*	Flow Control	Packet Size *(bytes)*	Packet Throughput *(kbit/s)*		
0x000E	0x0010	1	Disable	196	1000		
Continuous Test	Test Duration *(pkts)*	Packet Counter	Pattern Type				
Disable	10.000	Enable	Byte Counter				

Table 8-105: mitb_t5643_6pin_2048fs_casi (Part 2)

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8.7 Miscellaneous Tests

The following table provides an overview of available miscellaneous tests.

Overview Misc Tests	
Test Name	**Test Characteristics**
MediaLB 3-pin Tests	
mitb_t9330_3pin_1024fs_m_syscmd	1024xFs test with generation of system commands - MediaLB Port open without any Channel Addresses - No data transfer - MOSTLock, MOSTUnLock and MLBReset commands generated one after the other with a 2 second gap in between
MediaLB 6-pin Tests	
mitb_t9640_6pin_2048fs_m_syscmd	2048xFs test with generation of system commands - MediaLB Port open without any Channel Addresses - No data transfer - MOSTLock, MOSTUnLock and MLBReset commands generated one after the other with a 2 second gap in between

Table 8-106: Miscellaneous Test Overview

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8.7.1 mitb_t9330_3pin_1024fs_m_syscmd

Test Name	*mitb_t9330_3pin_1024fs_m_syscmd*						
Description	1024xFs test with generation of system commands - MediaLB Port open without any Channel Addresses - No data transfer - MOSTLock, MOSTUnLock and MLBReset commands generated one after the other with a 2 second gap in between						
Test Configuration Files	*mitb_t9330_3pin_1024fs_m_syscmd_cfg_setup.txt* *mitb_t9330_3pin_1024fs_m_syscmd_cfg_start.txt*			Manual setup of test via GUI possible?	YES		
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	3-Pin	1024xFs	none	PC0	0x01FE		
				PC1	0x0000		
				PC2	0x0000		
				…	…		
				PC31	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	3-Pin	1024xFs	0101h				
System Command Test Tab							
System Command	No. System Commands	Delay System Commands					
MOSTLock, MOSTUnLock, MLBReset	5, 10, 1916	100, 10, 200					

Table 8-107: mitb_t9330_3pin_1024fs_m_syscmd

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8.7.2 mitb_t9640_6pin_2048fs_m_syscmd

Test Name	*mitb_t9640_6pin_2048fs_m_syscmd*						
Description	1024xFs test with generation of system commands - MediaLB Port open without any Channel Addresses - No data transfer - MOSTLock, MOSTUnLock and MLBReset commands generated one after the other with a 2 second gap in between						
Test Configuration Files	*mitb_t9640_6pin_2048fs_m_syscmd_cfg_setup.txt* *mitb_t9640_6pin_2048fs_m_syscmd_cfg_start.txt*				Manual setup of test via GUI possible?	YES	
DUT MediaLB Configuration							
Port Mode	Interface Mode	Clock Speed	Transferred Data Type	Physical Channel	Channel Address	Allocated Transfer	
Device	6-Pin	2048xFs	none	PC0	0x01FE		
				PC1	0x0000		
				PC2	0x0000		
				…	…		
				PC63	0x0000		
GUI Configuration							
Configuration Tab							
RS232 Port	DUT MediaLB Interface Mode	DUT MediaLB Clock Speed	DUT MOST Target Address				
User configurable	6-Pin	2048xFs	0101h				
System Command Test Tab							
MOSTLock	No. System Commands	Delay System Commands	MOSTUnLock				
MOSTLock, MOSTUnLock, MLBReset	5, 10, 1916	100, 10, 200					

Table 8-108: mitb_t9640_6pin_2048fs_m_syscmd

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9 Summary of Provided Files

A description and the location of the files required to use the MITB and to verify a MediaLB device implementation can be found in the following sections.

9.1 Graphical User Interface Executable

The MITB GUI can be found on the provided installation CD in the following folder:

- *Software\MITB_GUI\V02_XX_YY*

This folder incorporates the following installation file:

- *MITB_GUI_V02_02_00_Installer.exe*

To install the GUI, double click on the file and follow the instructions.

When the GUI is executed the file *MITB_GUI_Parameters.ini* is generated. Parameters entered on the GUI are stored in this file when the GUI is closed and re-loaded, when the GUI is started again.

9.2 PCFlasher Executable

The PCFlasher application used to flash FPGA images and Pattern Generation & Analyzer firmware to the MITB platform can be found on the provided installation CD in the following folder:

- *Software\PCFlasher\V01_XX_YY*

This folder incorporates the following installation file:

- *PCFlasher_V01_01_01_Installer.exe*

To install the PCFlasher, double click on the file and follow the instructions.

9.3 FPGA Image

The following FPGA image is provided on the installation CD and can be flashed to the XILINX Virtex-4 FPGA on the MITB platform:

- *Firmware\MITB\V02_XX_YY\ SP89420_vhdl_v02_02_13-01_bootloader_v00_05_08-01.xsvf*

Hint The delivered MITB platform is by default flashed with the proper FPGA image. The FPGA needs to be flashed only in case a version update is required.

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9.4 Pattern Generator & Analyzer Firmware

The following Pattern Generator & Analyzer firmware is provided on the installation CD and can be flashed to the MITB platform:

- *Firmware\MITB\V02_XX_YY\MITB_PGA_V02_02_00-01.srec*

Hint The delivered MITB platform is by default flashed with the proper Pattern Generator & Analyzer firmware. The PGA needs to be flashed only in case a version update is required.

9.5 OS81110 INIC Firmware

The following OS81110 INIC firmware files are provided on the installation CD and can be flashed to the OS81110 devices part of the MITB:

- *Firmware\MITB\V02_XX_YY\OS81110_V01_02_03.ipf*:
  Intended to be flashed on OS81110, connected to PGA on MITB
- *Firmware\DUT\V02_XX_YY\MITB_OS81110_V00_90_XX_3pin.ipf:*
  Intended to be flashed on OS81110, connected to MDUT in case of MediaLB 3-pin testing
- *Firmware\DUT\V02_XX_YY\MITB_OS81110_V00_90_XX_6pin.ipf:*
  Intended to be flashed on OS81110, connected to MDUT in case of MediaLB 6-pin testing

Hint The MITB delivery incorporates three Phy+ Boards. The OS81110 devices assembled on these boards are by default flashed with the proper firmware.

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9.6 Test Configuration Files

The test cases defined in chapter 7 are grouped in categories. The following categories and folders are available on the installation CD:

- *Firmware\Testbench\V02_XX_YY\async*
- *Firmware\Testbench\V02_XX_YY\combined*
- *Firmware\Testbench\V02_XX_YY\control*
- *Firmware\Testbench\V02_XX_YY\isoc*
- *Firmware\Testbench\V02_XX_YY\misc*
- *Firmware\Testbench\V02_XX_YY\sync*

For every test case an additional sub-folder is available which incorporates configuration files defining test specific parameters. These configuration files can be loaded on the MITB GUI (by clicking “Load Config File” button) to execute a test case.

Two types of test configuration files are available:

- **Configuration setup files** and
- **Configuration start files**

The prefix (*mitb_txxxx_..._*) of a configuration file represents the test name.

Configuration setup files define general test parameters and have the following format:

mitb_txxxx_..._cfg_setup.txt

Configuration start files are used to start the pattern generation and the format looks as follows:

mitb_txxxx_..._cfg_start.txt

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Appendix A: References

[1] INIC Explorer User Manual, SMSC, http://www.smsc-ais.com/INIC_Explorer_Download
[2] MediaLB Analyzer User Manual, SMSC. http://www.smsc-ais.com/MediaLB_Analyzer_Download
[3] Physical+ Interface Board OS81110/2+0 Data Sheet, SMSC. Contact: support-ais-de@smsc.com
[4] MediaLB Specification V4.2, SMSC, http://www.smsc-ais.com/MediaLB_Download
[5] OS81110 Hardware Data Sheet, SMSC. Contact: support-ais-de@smsc.com
[6] OS81110 INIC API User's Manual, SMSC. Contact: support-ais-de@smsc.com
[7] OSS Flasher, SMSC, http://www.smsc-ais.com/OSS_Flasher_Download
[8] www.smsc.com

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Appendix B: List of Abbreviations

The table below gives an overview of abbreviations mentioned in this user manual, listed in alphabetical order.

Abbreviation	Definition
FOT	Fiber Optic Transceiver
GUI	Graphical User Interface
MDIM	MediaLB Device Interface Macro
MDP	MOST Data Packets
MDUT	MediaLB Device Under Test
MEP	MOST Ethernet Packets
MITB	MediaLB Interface Test Bench
PGA	Pattern Generator & Analyzer
Phy+ Board	Physical+ Interface Board OS81110

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Appendix C: Spare Part List

The following spare parts are available for this SMSC product.

Part Name	Part Number
Optical fiber set Yazaki 2+0	X10166
MOST150_oPHY_2+0 PHYplus Interface Board Variante1	X13363
MOST150_oPHY_2+0 PHYplus Interface Board Variante3	X13365
Powersupply_12V_3A5_TR45_Binder_V01_00_00	X13167
RS232 Interface Cable	X10162
USB-RS232 Adapter FTDI	X13179

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